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Military EMBEDDED SYSTEMS

VOLUME 5 NUMBER 2
MAR/APR 2009

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OpenVPX controversy brews

Duncan Young
Core 2 Duo magnifies VME

John Wemekamp
JPEG2000 ramps up digital video

Guest Column
QNX Software Systems
Non-scary multicore migration

Legacy software: Still flying high

Also:

Case study: Direct spray cools avionics boards

MicroTCA digs in on the modern battlefield

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ON THE COVER:
A B-52 Stratofortress leads a formation of Japanese Air Self Defense Force F-2s, U.S. Air Force F-16 Fighting Falcons, and a U.S. Navy EA-6B Prowler over Guam on Feb. 10, 2009. There is no better poster child for "legacy software" than the Old Buff, which started flying in the 1950s and remains in active service running DoD and COTS software. Today, that code is characterized as "legacy" but still requires upgrades and system modifications. Refer to our cover story on keeping legacy software viable and functional, page 16. (U.S. Air Force photo by Master Sgt. Kevin J. Gruenwald, courtesy of U.S. DoD DefenseLink)

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Ruggedized MicroTCA – with Conference Concepts
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PCI EXPRESS PENTEK 4207 NO DELAY
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Departures
Destination Board Model Status
PCI-X PENTEK 4207 NO DELAY
VXS PENTEK 4207 NO DELAY
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Introducing the One Board
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Military & Aerospace Group

Chris Ciufo, Group Editorial Director
cciufo@opensystemsmedia.com

Don Dingee, Contributing Editor
ddingee@opensystemsmedia.com

Jennifer Hesse, Senior Associate Editor
jhesse@opensystemsmedia.com

Sharon Schnakenburg, Associate Editor
sschnakenburg@opensystemsmedia.com

Terri Thorson, Senior Editor (columns)
tthorson@opensystemsmedia.com

Monique DeVoe, Copy Editor

Hermann Strass, European Representative
hstrass@opensystemsmedia.com

Konrad Witte, Senior Web Developer

Steph Sweet, Creative Director

Joann Toth, Senior Designer

David Diomede, Art Director

Phyllis Thompson
Circulation/Office Manager
subscriptions@opensystemsmedia.com

Sales Group

Dennis Doyle, Senior Account Manager
ddoyle@opensystemsmedia.com

Tom Varcie, Senior Account Manager
tvarcie@opensystemsmedia.com

Doug Cordier, Account Manager
dcordier@opensystemsmedia.com

Andrea Stabile
Advertising/Marketing Coordinator
astabile@opensystemsmedia.com

Christine Long, Digital Content Manager
clong@opensystemsmedia.com

International Sales
Dan Aronovic, Account Manager – Israel
daronovic@opensystemsmedia.com

Sam Fan, Account Manager – Asia
sfan@opensystemsmedia.com

Regional Sales Managers
Ernest Godsey, Central and Mountain States
egodsey@opensystemsmedia.com

Barbara Quinlan, Midwest/Southwest
bquinlan@opensystemsmedia.com

Denis Seger, Southern California
dseger@opensystemsmedia.com

Sydele Starr, Northern California
sstarr@opensystemsmedia.com

Ron Taylor, East Coast/Mid Atlantic
rtaylor@opensystemsmedia.com

Reprints and PDFs

Nan Lamade
800-259-0470
license@opensystemsmedia.com

Editorial/Business Office

16626 E. Ave of the Fountains, Ste 203
Fountain Hills, AZ 85268
Tel: 480-967-5581 ■ Fax: 480-837-6466
Website: www.opensystemsmedia.com

Publishers: John Black, Michael Hopper, Wayne Kristoff

Vice President Editorial: Rosemary Kristoff

Vice President Marketing & Sales:
Patrick Hopper
phopper@opensystemsmedia.com

Business Manager: Karen Layman

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Field Intelligence

VMEbus supports 64-bit Core 2 Duo processors

By Duncan Young

Contrary to many industry pundits' gloomy predictions, VMEbus continues to survive and flourish. The simple reason is that it still offers real value, whether this is measured in cost, time, performance, or its unique blend of functionality for many new applications. In addition, it provides the most cost-effective upgrade path for the very large base of existing VME implementations, in both industrial and military systems. VME has managed to maintain backward compatibility through its extraordinarily long lifetime, preventing its market from becoming fragmented by customers exploring other options. Embedded applications are now realizing the performance and ease-of-use benefits of Intel's Core 2 Duo processors which, when combined with the extensive and flexible I/O capability possible within the VME profile, extends VME's potential to a much broader application base.

Support of embedded applications

The Intel x86 family has not been first choice for real-time, embedded military applications due, in part, to commercial decisions made during the early years of COTS adoption. High power dissipations of certain devices have also demonstrated unfavorable MIPS-per-watt comparisons when implemented within the constraints of VME and other similar modular systems. As a result, the x86/Pentium was never featured as the primary processor choice for VMEbus systems. However, the commercial environment that prompted those earlier decisions has gradually swung back toward longer product life cycles and support of embedded applications; this, in turn, makes VMEbus a market to be taken seriously. In addition, the new 45 nm process technology of Intel's T9400 Penryn family of Core 2 Duo devices now provides 64-bit, dual-core processors clocked at 2.53 GHz and a 1,067 MHz front side bus with an overall power dissipation of 35 W: well within the power dissipation envelope of VME.

Although unlikely to challenge the dominant position of Freescale's e-600 core-based PowerPC line in the military's critical, real-time, and signal processing applications, the x86/Pentium is well established in infrastructure projects such as logistics and battle management. It is additionally deployed in embedded form in combat systems, test equipment, simulation, and training systems. Compared to many prepackaged, commercial alternatives, VME-based products still offer the greater choice of I/O capability and performance. The primary reason is that VME is supported by an industry infrastructure honed to the needs of the embedded developer, including vital longevity of supply and support. Many small form factor products, such as MicroTCA or PC/104, might seem to offer a more economical alternative at first sight but they tend to be I/O or performance bound. Often the addition of all the required capabilities results in overall system size and costs that compare badly to a VME alternative.

The wealth of I/O capability traditionally offered by VMEbus products has been further boosted by the widespread introduction of PCI Express, rapidly displacing PCI and PCI-X as the preferred form of I/O connection. PCI Express provides significant board real estate and routing savings, with the capability to be routed to PMC/XMC mezzanine expansion sites offering greater flexibility and performance for the latest generation of SBCs. PCI Express can also be used for board-to-board expansion, adding more PMC/XMC sites within the two-slot envelope of just an SBC and an adjacent expansion board.

Even though VME has so many associated standards for connecting fabrics, mezzanines, and I/O, it continues to offer scope for competitive differentiation of processor cards. The x86/Pentium SBCs must, of course, offer basic PC functionality, BIOS, and Windows support as necessary prerequisites. However, vendors will eternally innovate to achieve additional flexibility, performance, or I/O channels in their latest products. This is illustrated by the V7875 Core 2 Duo SBC from GE Fanuc Intelligent Platforms shown in Figure 1. It includes support for the VXS (VITA 41.3) switched data plane using GbE and has a unique PCI Express extension capability to add three PMC/XMC sites via an expansion board. This provides a site supporting 16-lane PCI Express intended for demanding graphical applications such as simulation and training that require high-performance, high-definition 3D rendering using advanced graphics engines such as ATI's Radeon E2400.

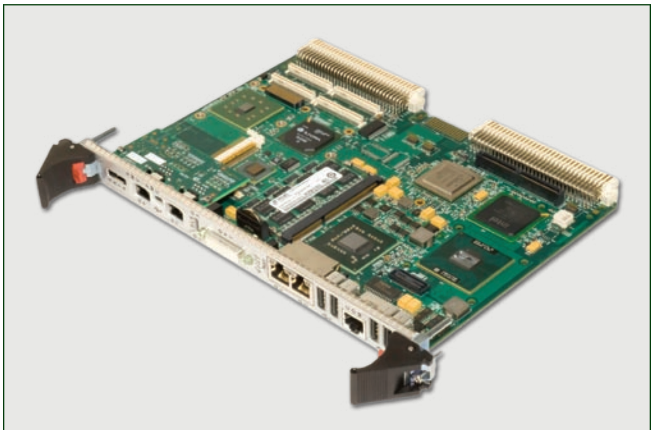

FIGURE 1: VME continues to offer scope for competitive differentiation of processor cards, but vendors will eternally innovate to achieve additional flexibility, performance, or I/O channels in their latest products.

The T9400 Core 2 Duo Penryn family offers an ideal processor platform for new VMEbus product development. It provides unmatched 64-bit performance for the vast majority of applications. It also provides power consumption and longevity of supply and support that are firmly aligned with the needs of the VME and military communities. Meanwhile, the Core 2 Duo appears set for more widespread adoption in future military embedded programs.

To learn more, e-mail Duncan Young at young.duncan1@btinternet.com.

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Mil Tech Insider

JPEG2000 cuts delays in digital video distribution

By John Wemekamp

Digital video distribution is a major growth area – and not just on traditional surveillance platforms such as naval combat systems, maritime patrol aircraft, or armored scout vehicles. Digital distribution removes the straitjacket of wired analog distribution, with discrete cables per video source, enabling video to be distributed over multiple carriers over long distances and at high quality and high resolutions. In addition, many armored vehicles are now being equipped with local situational awareness systems offering all-around vision with the hatches closed. These vehicles may also receive downlinked images of the battlefield from Unmanned Aerial Vehicle (UAV) sensors in real time.

Digital video applications

The most common applications are large, multisensor platforms with many crew stations, each one potentially able to view any-from-many video sources on one or several screens simultaneously. Distribution of analog video requires considerable cabling plus complex switching and scaling hardware at each crew station. The complexity of such systems is magnified by the recent introduction of higher-resolution, point-to-point digital video/audio interfaces with their restricted transmission distances and cable routing issues. These include the PC standards such as High-Definition Multimedia Interface (HDMI) found in modern flat-panel TVs and monitors. Some military applications achieve uncompressed digital video transmission using the ARINC 818 standard, which is based on Fibre Channel signaling (specifically FC-AV). Video compression and distribution as IP packets over an Ethernet network is a solution being adopted for large platforms. The same principles are being applied to many smaller platforms with multisensor payloads that may be required to share data and images externally across the digital battlefield.

However, compression can cause loss of clarity and detail and introduce delays into signal paths. Delay is usually unacceptable when used for fire direction or for driving a ground vehicle, making the choice of compression algorithm critical. The most familiar standards for video compression, MPEG-2 and MPEG-4, add delays of typically 300 mS by using multiple frames to discriminate changes. There may also be a loss of picture integrity plus some additional recovery time if one frame is lost or corrupted during transmission. The alternative is to use frame-by-frame compression of JPEG2000, where coding and decoding operate at frame rate and any delays are limited to transmission times through a network. JPEG2000 also offers selectable compression ratios for optimum use of bandwidth. For example, with a typical compression ratio of 30:1, TV rate video only requires a bandwidth of 1 Mbps through a network.

Managing costs and distribution

JPEG2000 is appropriate for all types of video distribution, offering better quality and response at similar overall cost compared to MPEG. One example where the solution is often strongly dictated by budget is local situational awareness in an armored vehicle. This uses a number of cameras at TV resolution and will require little image processing. A typical configuration is for each camera to incorporate JPEG2000 compression, hooking up directly to the vehicle's local network and using onboard embedded computing resources to decompress and display the images on one or two local displays. By using embedded computing resources, images and annotations added by the crew could also be distributed externally through radio or satellite links to command posts or to other vehicles on the ground. Larger platforms such as naval combat systems or surveillance aircraft will host more complex applications requiring additional image or display processing; these include target tracking, identification, and classification; sensor fusion; and windowing. The image processing will be more closely integrated with many embedded computing systems and will deal with video of much higher quality. This application will distribute not only compressed sensor video via the network, but it will also have many cooperative participants sharing processed/synthetic video from many sources (for example, from one combat system display console to many others).

JPEG2000 is now a well-accepted standard for high-quality video distribution, particularly in embedded systems modules such the Orion JPEG2000 PMC module from Curtiss-Wright Controls Embedded Computing (CWCEC) shown in Figure 1. Technology improvements are set to greatly improve packaging and performance of this class of product; PCI Express is replacing older PCI and PCI-X parallel interfaces. Secondly, an FPGA can now be used for real-time JPEG2000 compression and decompression on multiple channels at HD resolutions and beyond, up to 1,920 x 1,200. These improvements make it possible to implement capability onto just a single XMC/PMC module, compatible with off-the-shelf embedded computing standards, to support DVI as well as PAL/NTSC sensor and display video streams. In addition, such a module could operate as a JPEG2000 coprocessor for the interplatform, console-to-console, or platform-to-platform class of video distribution.

Moving compressed video as IP packets through a network saves space, weight, and cost by making more efficient use of what is often underutilized existing infrastructure. The new generation of JPEG2000 products provides the capability to incorporate HD levels of video resolution with the compression ratios and video quality to match current and future network, sensor, and display performance.

To learn more, e-mail John at john.wemekamp@curtisswright.com.

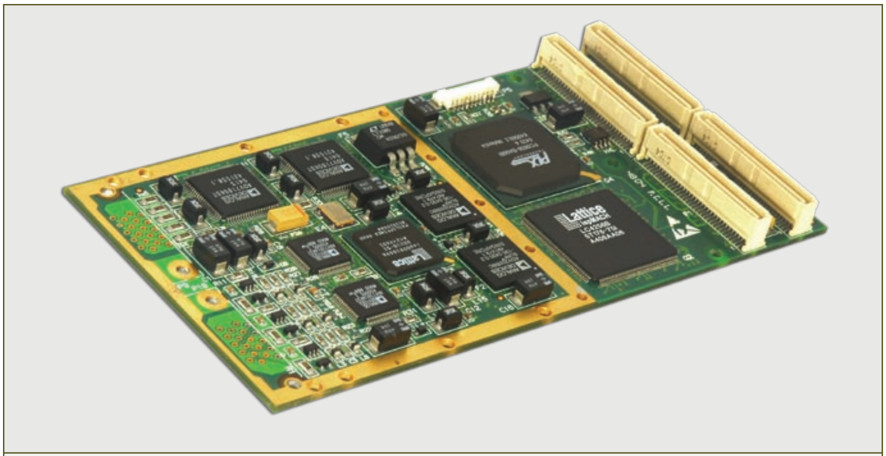


FIGURE 1: JPEG2000 is now a well-accepted standard for high-quality video distribution, particularly in embedded systems modules such Curtiss-Wright's Orion JPEG2000 PMC module.

Daily Briefing: News Snippets

By Sharon Schnakenburg, Associate Editor

www.mil-embedded.com/dailybriefing

GPU computer sales plummet – Q4'08

They're high, they're low. They're fast, then they're slow. What are they? 2008 shipments of GPU-equipped computers, according to a recent report by graphics research firm Jon Peddie Research (JPR). First the good news: Q3-2008's tallies were atypically high, even for oft-successful third quarters. The bad news: Total GPU shipments for Q4-2008 hit a sluggish 72.35 million, a significant decline from the 111.26 million shipped in Q3-2008 and 100.5 million in Q4-2007. Consequently, AMD, Intel, and NVIDIA market shares decreased between Q3-2008 and Q4-2008 (Table 1). Meanwhile, desktop sales dropped 39.5 percent and notebook shipments decreased 29 percent between the third and fourth quarters of 2008. Dr. Jon Peddie, JPR president, says, "We're forecasting a strong Q3 and Q4 for 2009 and bracing for what will probably be the worst Q1 and Q2 decline we've seen since the Internet bubble pop of 2000."

Vendor	Q3-2008	Market share	Q4-2008	Market share
AMD	22.90	20.6%	14.00	19.3%
Intel	54.95	49.4%	34.59	47.8%
NVIDIA	30.93	27.8%	22.20	30.7%

Table 1: Source: JPR

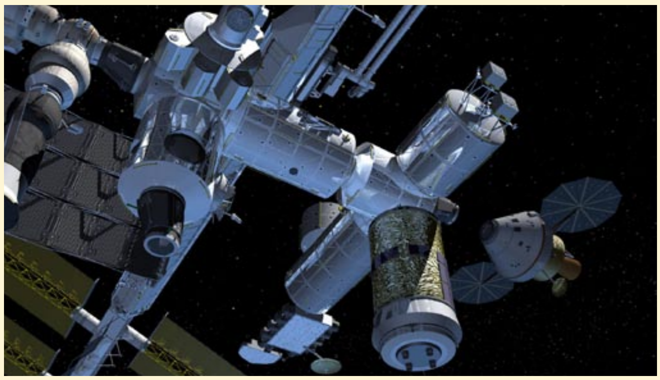
'Avenger' system defies old-time smoke screens

While old TV and movies depict smoke screens as the best tactical maneuver in avoiding enemy detection, Boeing has successfully completed testing on a high-tech alternative: the Laser Avenger laser system. Laser Avenger fires a laser beam at enemy UAVs without the gun flashes or missile exhaust produced by traditional weapons that can reveal troops' locales. While a 2007 demonstration of the laser system confirmed its ability to neutralize Unexploded Ordnance (UXO) and IEDs, recent tests conducted at White Sands Missile Range in New Mexico – and observed by U.S. Army Cruise Missile Defense Systems reps – showed Laser Avenger combat-vehicle capable of UAV disablement. To ready Laser Avenger for its recent exams, laser power was doubled, the design ruggedized and simplified, and sophisticated pointing and tracking capability added – all within less than one year, Boeing reports.

Photo courtesy of Boeing

NASA's Orion takes hands-off approach

It would seem logical to have hardware physically present to develop it, modify it, or integrate it into a system – unless one uses a virtual platform. Case in point: Honeywell's recent selection of Virtutech's Simics virtual platform for NASA's Orion spacecraft. Touted to reduce hardware iterations by one-half, Simics will provide a software development platform nearly a year before the crew exploration vehicle's hardware is physically available. The Simics full systems simulator's capabilities include resuming/saving execution, reverse and forward execution, fault injection, full deterministic behavior, and noninvasive debug and trace, among others. Lockheed Martin is prime on Orion, which will transport crew members to the moon, the International Space Station, and someday Mars.



Artist rendering courtesy of NASA

Laser pulses: Not the speed of light

Though the speed of light was quantified long ago, the speed of laser pulses is still up for debate. However, a recent Phase II Small Business Technology Transfer (STTR) contract for $500,000 between the Naval Air Warfare Center (NAVAIR) and "ultrafast" laser producer Raydiance, Inc. aims to solve the ambiguity. The contract furthers the work recently finished in Phase I, surrounding the ongoing development of new fiber technology that can be used to transmit "high-power Ultrashort Pulse (USP) or 'ultrafast' lasers over fiber." The new technology's target: NAVAIR apps including Electronic Countermeasures (ECM), LiDAR, and explosives detection, among others. Phase II finds Raydiance renewing its Phase I collaboration with MIT in enhancing the ultrafast laser's weight, form factor, capabilities, and cost.

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USAF thwarts critical interruptions

Getting interrupted during a conversation can prove highly annoying to civilians. But an interruption in battlefield communications can prove much more frustrating – and even deadly. Accordingly, the U.S. Air Force commissioned Thales Communications to provide more than 700 of its 50-watt AN/VRC-111 Vehicle Adapter Amplifier (VAA) systems, along with more than 200 20-watt AN/VRC-111 systems for the USAF's Tactical Air Control Party Modernization Office (TACP-M). With several deliveries to Hanscom Air Force Base recently completed, each VAA includes dual AN/PRC-148 JTRS Enhanced Multiband Inter/Intra Team Radios (JEMs), rendering cable-free, fast radio dismount in under two seconds with no communications loss. The two-channel AN-VRC-111 VAA is an SDR-based system providing 50 W at frequencies of 30 to 88 MHz, or 20 W at frequencies of 90 to 512 MHz. The AN-VRC-111 system, on the other hand, provides 20 W at frequencies of 30 to 512 MHz.

LM stays ahead of the curve

Lockheed Martin (LM) recently earned – five years earlier than required – the Italian Ministry of Defense's (MoD's) "industrial benefit requirement" signoff surrounding the acquisition of twenty-two C-130J airlifters. The industrial benefit requirement includes a broad spectrum of Italian companies and comprises initiatives such as license establishment, technology transfers, and LM's direct investment in Italian industry. Italy's Aeronautica Militare was one of the original C-130J customers in 1997, and its pilots have logged more than 75,000 flight hours thereon. The C-130J airlifter was developed to fulfill missions ranging from air-to-air refueling, to disaster relief, combat delivery, special operations, and more.

Open source database reduces unknowns

In association with a contract with the U.S. Department of Homeland Security, Coverity announced recent publication of its for-public-use online "Scan" database of application architectures. Scan contains data "compiled" from more than 2,500 open source projects (www.scan.coverity.com), gathered via the Coverity Architecture Analyzer. The website features software data from Postfix, Samba, Perl, Amanda, OpenPAM, TCL, NTP, Overdose, and Python, among many others. Scan helps reduce design issues by enabling comparison of an architecture to various code bases, lending developers increased structural understanding. Scan also assists designers who are developing a module or plug-in by ensuring that the design meshes with expectations relevant to the target open source project.

Largest investment to produce smallest technology

In what is purported as Intel's "largest-ever investment for a new manufacturing process," the company will invest $7 billion to build U.S. "advanced manufacturing facilities" to produce its smallest offering: 32 nm technology. The investment's designated locations in Arizona, Oregon, and New Mexico are earmarked to support about 7,000 high-skill, high-paying positions. "We're investing in America to keep Intel and our nation at the forefront of innovation," Intel CEO and President Paul Otellini said in a statement to the media. First up in Intel's upcoming 32 nm plan is the "Westmere" processor, which melds Nehalem technology with integrated graphics capabilities and is scheduled to begin production this year.

Software companies experience economic gains

In contrast to the downward spiral many industries and companies are experiencing, two software companies are reporting growth: Middleware specialist Real-Time Innovations (RTI) claims "record revenue for the seventh consecutive year" and a Compounded Annual Growth Rate (CAGR) of more than 44 percent for its core middleware offerings. International design wins, up by 80 percent from 2007, were among the primary growth factors. In addition, Tensoft, Inc. announced an increase in software revenue of 100 percent in 2008. Tensoft CEO Bob Scarborough credits a solid customer base and partnership with Microsoft as key to Tensoft's 2008 success.

U.S. Army 'virtually' scores accolades

In 2002, the U.S. Army released its America's Army PC game to give civilians virtual experience in soldiering on battlefields and in barracks. Its developers were even required to discharge weapons, conquer obstacle courses, participate in combat training, and observe paratrooper instruction to lend as much realism as possible. Those taking note include the game's 9.7 million registered users (or "virtual army") as well as the Guinness World Records organization. Accordingly, the 2009 Guinness Gamer's Edition will grant America's Army five awards: Largest Virtual Army; Most Downloaded War Video Game (42.6 million downloads); Most Hours Spent Playing a Free Online Shooter (230.9 million hours); Earliest Military Website to Support a Video Game (www.americasarmy.com); and Largest Traveling Game Simulator – Virtual Army Experience accommodates as many as 50 players. America's Army version 3.0 is set for release this year.

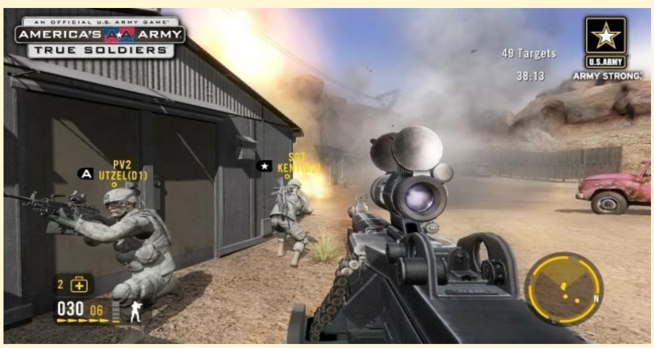

Photo courtesy of U.S. Army. Soldiers in "America's Army: True Soldiers" attack an enemy encampment in the fictional country of Ganzia. The player controls the weapon in the foreground. Before using a weapon in combat, players must meet Army training standards.

Legacy Software Migration

By Bill Graham

Migrating legacy applications to multicore: Not as scary as it sounds

Multicore processors bring significant performance and power usage benefits to embedded systems, but they also add the complexity of multiprocessing to the legacy migration workload. Nonetheless, development teams can successfully manage their transition to multicore by following some straightforward techniques.

Port to a portable standard

Often, migrating to multicore involves more than moving to a new processor. In many cases, developers must first port the legacy code to a new programming language, compiler, or OS. Using an open standard such as POSIX is highly recommended, in light of its support of many general-purpose and real-time operating systems. Doing so will help ensure that large portions of the application, including its interface with the OS, are portable. Just as important, the POSIX standard has a proven history in multiprocessing systems, and a multicore processor is simply a multiprocessing System-on-Chip (SoC).

Divide and conquer

The OSs that support Symmetric Multiprocessing (SMP) are the best option for homogenous multicore processors. SMP leaves the complex details of allocating CPU resources to the OS, rather than to the application. From the application's point of view, the interface to the OS remains the same, regardless of the number of cores, from 1 to N. Consequently, the application can scale easily as more cores are added.

A multicore system running in SMP mode provides true parallelism, but some legacy applications were never designed for parallel execution. Often, large portions of the code do not use threads, which would allow different parts of the application to run in parallel or use threads only to isolate blocking system calls such as file or network I/O.

Another typical pitfall occurs when code uses a priority scheme to control access to shared memory. For instance, in a uniprocessor embedded system, the software developer can often assume that a high-priority thread and a low-priority thread will not access the memory simultaneously, since the high-priority thread will always preempt the low-priority thread. Thus, many programs fail to use a mutual exclusion lock (mutex) to properly synchronize access to the memory. In an SMP multicore system, however, both of these threads can run in parallel and, as a result, access memory simultaneously with unpredictable results. Other insidious problems might exist due to synchronization errors that work perfectly on a single processor system but surface only in multiprocessor execution.

"... Insidious problems might exist due to synchronization errors that work perfectly on a single processor system but surface only in multiprocessor execution."

To solve such problems, developers can divide and conquer: isolate the problem code on a single core of the multicore chip until the code can be fixed. To do this, developers can use Bound Multiprocessing (BMP), an extension to SMP that allows selected processes to run on only a specified core or CPU. In effect, BMP provides a single-core, nonparallel execution environment for legacy code while allowing other code to leverage the full parallelism of SMP. The development team can subsequently remove the CPU binding once they have modified the legacy code to behave properly in its new parallel environment.

Leverage the tools

Development teams must also use the right tools. In particular, they need visualization tools that help them pinpoint areas where code is misbehaving in a parallel environment. Mostly, this effort involves the detection and correction of the synchronization bugs mentioned earlier.

Once an application is operating properly, it may still fail to take advantage of all of the multicore chip's CPU capacity. Visualization tools can help here, too, by allowing developers to reduce contention for shared resources (hot spots), eliminate excessive thread migration or communication between cores, and find opportunities for parallelizing code. As the number of cores increases in multicore platforms, visualization tools will be the key to successfully leveraging the performance benefits that multicore offers.

To provide such analysis, multicore visualization tools must reach beyond the scope of conventional debug tools. They must, for example, track threads as they migrate from one core to another and diagnose messages flowing between cores. They must also offer flexible control over which events are recorded and when, so that developers can focus on areas of concern.

Making the transition

"Multicore" does not need to be a bad word nor add another roadblock to legacy migration. Adopting portable programming standards such as POSIX, using OSs designed for multicore platforms, isolating legacy code to run on a single core, and using visualization tools all make the transition less daunting.

***Bill Graham** is product marketing manager at QNX Software Systems. He has more than 20 years of experience in the software industry, including embedded and real-time systems development, software development processes and techniques, UML modeling, and object-oriented design. He holds Bachelor's and Master's degrees in Electrical Engineering from Carleton University in Ottawa, Canada. He can be reached at bgraham@qnx.com.*

787 "Dreamliner" photo courtesy of Boeing

'Legacy' is not a four-letter word

By Robert Dewar

Though "legacy" code is often viewed negatively, it is proving itself a success in modern apps, thanks to its benefits of increased reliability and reduced effort. Two key aspects of this code reuse include developing reusable code and choosing appropriate legacy code.

I am often asked whether any new applications are being started from scratch in Ada. There are indeed some examples, a notable one being iFacts[1], a land-based component of the new air traffic control system for the United Kingdom's National Air Traffic Services (NATS). This application is being developed in Ada, using the SPARK dialect with rigorous formal methods. However, that project is an exception. Most new large applications are not started from scratch in Ada, or in any other language for that matter. Instead, they make varying use of so-called "legacy" components, reusing code from earlier systems.

The word "legacy" is perhaps ill-chosen. For many, it seems to denote rusty old junkware, and many programmers would clearly prefer to invent (and often reinvent) by writing new code. But "legacy software" can also mean effectively deploying reusable modules and systems, an obviously desirable goal.

There are many reasons why reuse beats writing new code. First, and most obviously, developing complex software is an increasingly expensive proposition, and anything that can reduce this effort and its associated costs is highly desirable. But perhaps even more importantly, tried-and-true code that has been effectively deployed is likely to be reliable.

Paths to reliable code

There are two rather different ways to demonstrate reliability for new applications. The first is to use powerful techniques that prevent defects from being introduced. The iFacts system exemplifies this approach. It is written almost entirely in SPARK (Figure 1) using mathematical proof techniques to ensure freedom from such defects as unanticipated arithmetic overflow or out-of-range array indices.

The use of formal methods will become more prominent as more applications have strenuous safety and security requirements. For example, the increased rigor associated with formal approaches helps developers address the higher levels of safety standards such as DO-178B[2] for commercial avionics. And the highest level of security in the Common Criteria[3], EAL7, actually requires fully formal techniques (Figure 2). The recently released Tokeneer system[4], a demonstration project sponsored by NSA and engineered using SPARK, illustrates this formal approach to ensuring freedom from defects. Tokeneer is a program that controls access to a secure enclave using biometric data. The project's goal is to show that it is feasible (and practical) to create such an application by formally proving the necessary security properties.

```
package Clock
  --# own in Ticks;
  is
    subtype Times is integer range 0 .. 86399;
    procedure Read (Time : out Times);
    --# global  in Ticks;
    --# derives Time from Ticks;
    --
    -- Time contains the number of seconds since the
    -- controller was powered up, and resets to zero
    -- every 24 hours
  end Clock;
```

FIGURE 1: The iFacts system, a land-based component of the new air traffic control system for the United Kingdom's National Air Traffic Services (NATS), is being developed in Ada, using the SPARK dialect with rigorous formal methods.

However, there is another path to reliability: long-term deployment of code in real-world systems. Over years of use, such strenuous testing can bring large systems to effectively converge to a state of impressive reliability. Examples are the Apache server[5], the PARS airline reservation system[6], and versions

EAL	Requirements
1	Functionally tested
2	Structurally tested
3	Methodically tested and checked
4	Methodically designed, tested, and reviewed
5	Semiformally designed and tested
6	Semiformally verified design and tested
7	Formally verified design and tested

FIGURE 2: The increased rigor associated with formal approaches helps developers address the higher levels of safety standards such as DO-178B for commercial avionics.

of the AIX operating system[7]. The latter is an interesting data point, since the iFacts application is built on top of AIX, and there would not be much point in creating a highly reliable application if the underlying operating system itself was not trusted. This trust comes not from a formal demonstration of correctness (which is beyond the state of the art), but from NATS experience in deploying AIX in live air traffic control systems for more than a decade. Of course, past performance is not a guarantee against bugs appearing in the future, but in the practical world of system development, with finite time and resources, there is good rationale for the position, “If it ain’t broke, don’t rewrite it.”

It seems obvious, then, that reusing legacy code is a good thing. However, many program managers almost seem to apologize for going this route. Interestingly, they might have some quite understandable rationale. Let’s look at two aspects of reuse that can cause problems if not handled carefully: developing reusable code and choosing appropriate legacy code.

Developing reusable code

How does one create reusable code in the first place? If a component is to be effectively reused, it must be written in a highly portable manner, since it will likely be redeployed in a different environment – one that uses a different architecture or compiler from the original. A software component’s portability depends on the chosen programming language and how the language’s features are used. Undefined or implementation-dependent behaviors are particularly problematic, and these vary across languages. For example, the effect of integer overflow is undefined in C, but many compilers have implemented “wraparound” treatment and many C programmers have come to rely on this as the expected behavior. The integer overflow’s effect is well-defined in Java (wraparound semantics, which might, however, cause other problems) and in Ada (raising an exception). Other potential sources of nonportability are data alignment and pointer size assumptions, compiler-dependent extensions, and target-system-specific libraries.

For effective reuse, program components must be well designed and documented. From an interface specification, programmers must be able to tell exactly what the code is supposed to do and how it should be (re)used. Equally important, internal comments must provide sufficient detail and be consistent with the code so that a programmer needing to modify the component years later can understand how it works. Designing for effective reuse definitely takes skill and can increase the expense and time required for the original implementation. Consequently, the extra benefits are potential and long term, but the additional costs are actual and short term. It is easy to understand why, faced with that tradeoff, software project managers are not rushing to make design for reuse one of their major priorities.

Choosing appropriate legacy code

The second vital factor in successfully reusing code is ensuring fitness-for-purpose. To benefit from well-used code’s reliability, code must be used correctly in its new context. Neglecting to follow this essential principle led to the spectacular destruction of the Ariane 5 rocket[8] during its initial launch. Some reused code from Ariane 4 caused a catastrophic system failure because the specifications for an important flight parameter of the new rocket did not match those of the earlier rocket. An unexpected out-of-range condition occurred during a conversion from floating point to integer, which led to a guidance system shutdown.

Fortunately, there are certainly also many instances of successful legacy software use. Payroll systems, typically written in COBOL, serve as an illustration. Tax laws change annually, often radically, but the design of parameterizable modular components obviates the need to rewrite these systems each year. Appropriate languages, programming styles, libraries, and management practices are crucial factors in such successful legacy code use.

In with the old, out with the new

Despite failures in some cases such as Ariane 5, proper legacy code reuse can reduce costs and increase reliability and safety. A recent highly visible example is the avionics system of the Boeing 787 "Dreamliner." (See photo, first page of this article.) Dreamliner is an all-new plane with all-new hardware technology and materials, but the software aboard has a significant proportion of reused modules from other Boeing airplanes. So when someone asks you, "What's new in your latest software system?" let's hope you can answer, "Same old, same old." Whether it's called "legacy code" or "reusable components," the benefits can be huge.

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***Dr. Robert Dewar** is cofounder, president, and CEO of AdaCore; he has also had a distinguished career as a professor of Computer Science at the Courant Institute of New York University. He has been involved with the Ada programming language since its inception in the early 1980s and, as codirector of both the Ada-Ed and GNAT projects, led the NYU team that developed the first validated Ada compiler. He has coauthored compilers for SPITBOL (SNOBOL), Realia COBOL for the PC (now marketed by Computer Associates), and Alsys Ada. He is also a principal architect of AdaCore's GNAT Ada technology. He has also written several real-time operating systems for Honeywell Inc. He can be reached at dewar@adacore.com.*

The full-length version of this article appears at www.mil-embedded.com/articles/id/?3729.

AdaCore
212-620-7300
www.adacore.com

Case study: Direct spray maximizes environmental isolation and flexibility on airborne platforms

By Andy Finch and Jeff Weiler

Military embedded systems experience harsh and rugged environments. In recent years, the power levels of the electronics deployed in these systems have been rising rapidly. The combination of the harsh environments with the rising heat loads of the electronics has forced vendors to develop more effective packaging technology. Meanwhile, direct spray cooling is proving itself an acceptable alternative to air and conduction cooling, providing exceptional environmental isolation and enabling lower lifetime cost of ownership. A case study is presented on Northrop Grumman's (NG's) Airborne Signals Intelligence Payload (ASIP), which includes a configuration of the direct spray cooled Multi-Platform Enclosure (MPE) and appears on NG's manned U-2 high-altitude reconnaissance plane and the Global Hawk UAV.

Existing and emerging applications running on military embedded systems are demanding ever-increasing computational power and communications bandwidths. For example, UAVs running signal intelligence systems or executing real-time image processing are driving impressive power densities at the board, chassis, and platform levels. Even more impressive are the demands created by radar processing systems, with system-level power consumption in the tens of kilowatts. At the same time, platform integrators are requiring smaller, lighter, and more efficient board and chassis-level products. Thus, platform integrators are forced to look for alternative cooling solutions.

A number of liquid-based cooling approaches exist. Most familiar to end users are conduction-cooled systems. In addition, the Liquid Flow Through (LFT) cooling approach is emerging, which typically uses PolyAlphaOlefin (PAO) as the coolant but differs from conduction cooling by delivering coolant to liquid-cooled cold plates mounted to components on the electronics[1]. Increasingly, direct spray is being viewed as an acceptable alternative to air and conduction cooling, providing excellent environmental isolation (Table 1) and enabling lower lifetime

Platform Requirements			
Temperature (°C)	-65 to +71		
Altitude (ft)	25,000-70,000		
Temperature Gradients	**Air**	**Conduction**	**Direct Spray**
ΔT°C ($T_{slot\ n} - T_{slot\ 1}$)	20	10	2
Enclosure			
Available Cooling Capacity (W/slot)	100	100[1]	500
Projected Enclosure Capability			
Cooling Capacity (W/slot)	200[2]	200[3]	850-1,000

[1]Industry data for conduction. Few applications achieve this power density.
[2]Industry data for Air Flow Thru (AFT) boards and enclosure
[3]Industry data for Liquid Cold Plate with conduction enclosure and boards

TABLE 1: Temperature requirements and cooling capacity comparison – Increasingly, direct spray is being viewed as an acceptable alternative to air and conduction cooling, providing excellent environmental isolation.

Multi-Platform Enclosure (MPE) for today's military embedded systems

It is critical to protect the payload electronics on military platforms from the effects of vibration, shock, sand, salt spray, and EMI, while simultaneously providing effective thermal management. The Multi-Platform Enclosure (MPE) shown in Figure 1 utilizes direct spray technology and is designed to provide environmental isolation from the harsh environments experienced during military use. Rugged or commercial-grade electronics can be housed inside the sealed enclosure, isolating electronics from sand, blowing dust, humidity, and many other undesirable operating conditions.

FIGURE 1: The Multi-Platform Enclosure (MPE) utilizes direct spray technology and is designed to provide environmental isolation from the harsh environments experienced during military use.

The MPE's predecessor was first developed for the Navy's EA-6B Prowler platform, specifically for the Prowler's aft power supply, to provide the necessary environmental isolation and thermal management. At the time of engagement with the Navy, the EA-6B's air-cooled aft power supply had a failure rate in the low 100s of hours. In preparation for flight testing, the power supply and its chassis were subjected to a full suite of MIL-STD testing, including catapult launches, arresting hook, shock, vibration, turbulence, and constant acceleration testing. In addition, the direct spray enclosure accumulated more than 400 hours of Prowler testing. By the conclusion of the testing, it was estimated that the MTBF of the aft power supply had risen by more than 1,900 percent (to 3,000 hours). In recent years, DoD adoption of the MPE has been accelerating, and the Global Hawk ASIP is a relevant example.

cost of ownership. These principles are illustrated in the following case study on the Airborne Signals Intelligence Payload (ASIP), to be installed on all Block 30 Global Hawk aircraft.

USAF Airborne Signals Intelligence Payload (ASIP)

ASIP, developed by Northrop Grumman (NG) for the U.S. Air Force, is the next-generation signals intelligence sensor. The system detects, identifies, and locates radar and other types of electronic and modern communication signals[2]. The sensor first flew on Global Hawk in 2005 and recently completed extensive qualification flights on the U-2 high-altitude reconnaissance plane.

FIGURE 2: The ASIP's enclosure, a configuration of the direct spray cooled MPE, is designed to environmentally isolate sensitive electronics and provide necessary thermal management.

Environmental isolation

Figure 2 shows the ASIP's enclosure, a configuration of the direct spray cooled MPE (see sidebar) designed to environmentally isolate the sensitive electronics and provide necessary thermal management. Flying on the U-2 or UAV, the payload housed in the unpressurized areas in the aircraft is subjected to extreme environmental conditions: temperatures as high as +70 °C at sea level and -65 °C at 70,000 feet.

The electronics packaging enabled by the direct spray system allows NG to field commercial grade electronics. Even in harsh environments, the commercial grade electronics successfully survive the rigors of the airborne platform. Typical ratings for fully rugged boards are in excess of 10 Grms and can be as high as 20 Grms. The vibration profile for Global Hawk is 2.5 Grms. Many of the electronics were only rated for 2.7 and 5.1 Grms sine profile from 15-2,000 Hz for operational and endurance profiles, respectively. Depending on the vehicle profile, stiffening ribs may be added to commercial cards. With the cost of fully rugged boards often double that of commercial grade electronics, significant life-cycle cost savings can be gleaned with less rugged cards.

Another intrinsic flexibility of direct spray enclosures is acceptance of varying heat densities. In ASIP, different card sets are used for applications ranging from 600 to 1,700 W in enclosure power, yet the enclosure is identical between all use cases. For diverse heat loads, an external heat exchanger easily scales with power densities. Heat rejection options include fuel, PAO, EGW, RAM air, ambient air, or skin/hull. Dependence on platform infrastructure for cooling options is eliminated as the direct spray enclosure and heat exchanger act as a self-contained system in pressurized or unpressurized environments.

Several ASIP cards are RF receiver cards tuned to between 20 and 3,000 MHz, while other cards range up to 18 GHz. With air-cooled systems, the electronics closest to the air supply are coolest while those near the air exhaust operate hotter. Conduction cards also create a thermal gradient from the middle of the enclosure to the first and last slots. Due to temperature sensitivity of the RF electronics, compensation is usually required between cards in the enclosure. NG took advantage of the innate ability of direct spray to limit the temperature gradient to less than 2 °C across a 20-slot system with power densities ranging from 30 to 60 W per board. In the ASIP enclosure, the electronics are maintained between +30 °C and +50 °C while the ambient temperature ranges from -65 °C to +71 °C.

> “NG took advantage of the innate ability of direct spray to limit the temperature gradient to less than 2 °C across a 20-slot system with power densities ranging from 30 to 60 W per board.”

Also, heat fluxes up to 50 W/cm² are found on bare die processors such as the 1.8 GHz Pentium M and are similar to those used in ASIP. With 70 °C inlet fluid, direct spray is able to maintain die temperatures at or below 90 °C. This is at least 10 °C lower than conduction-cooled enclosures. For electronics, it is widely accepted that for every 10 °C in temperature rise, reliability is reduced by 50 percent. The reliability impact of pumps, valves, and controllers is easily overcome by doubling the reliability of twenty 6U cards.

Efficient technology refresh means lower ownership costs

Integrators face the challenge of integrating air- and conduction-cooled boards on the same aircraft. Traditionally, it is not possible to mix electronics in the same enclosure due to constraints in both board and enclosure designs. For the ASIP sensor, NG was able to do just that by combining proprietary boards, commercial grade air-cooled SBCs, and other commercial Radio Frequency (RF) receiver cards into the enclosure. The enclosure consists of 20 user slots with inherent flexibility to mix and match electronics in unconditioned space and pressurized locations on the platform.

This electronics packaging technology enables smaller, lighter, power-efficient systems that can go through a technology refresh in a matter of months as opposed to years, providing for significantly lower total cost of ownership over the lifetime of the program.

Direct spray enclosures meet today's demands

The direct spray enclosures have been thoroughly evaluated for performance, reliability, and maintainability in harsh environments. The ability to protect sensitive electronics under extreme altitude, temperature, and vibration has been proven on platforms like U-2 and Global Hawk. The inherent flexibility in the selection of electronics enhances the utility of direct spray enclosures on legacy platforms and developmental aircraft, resulting in lower ownership costs.

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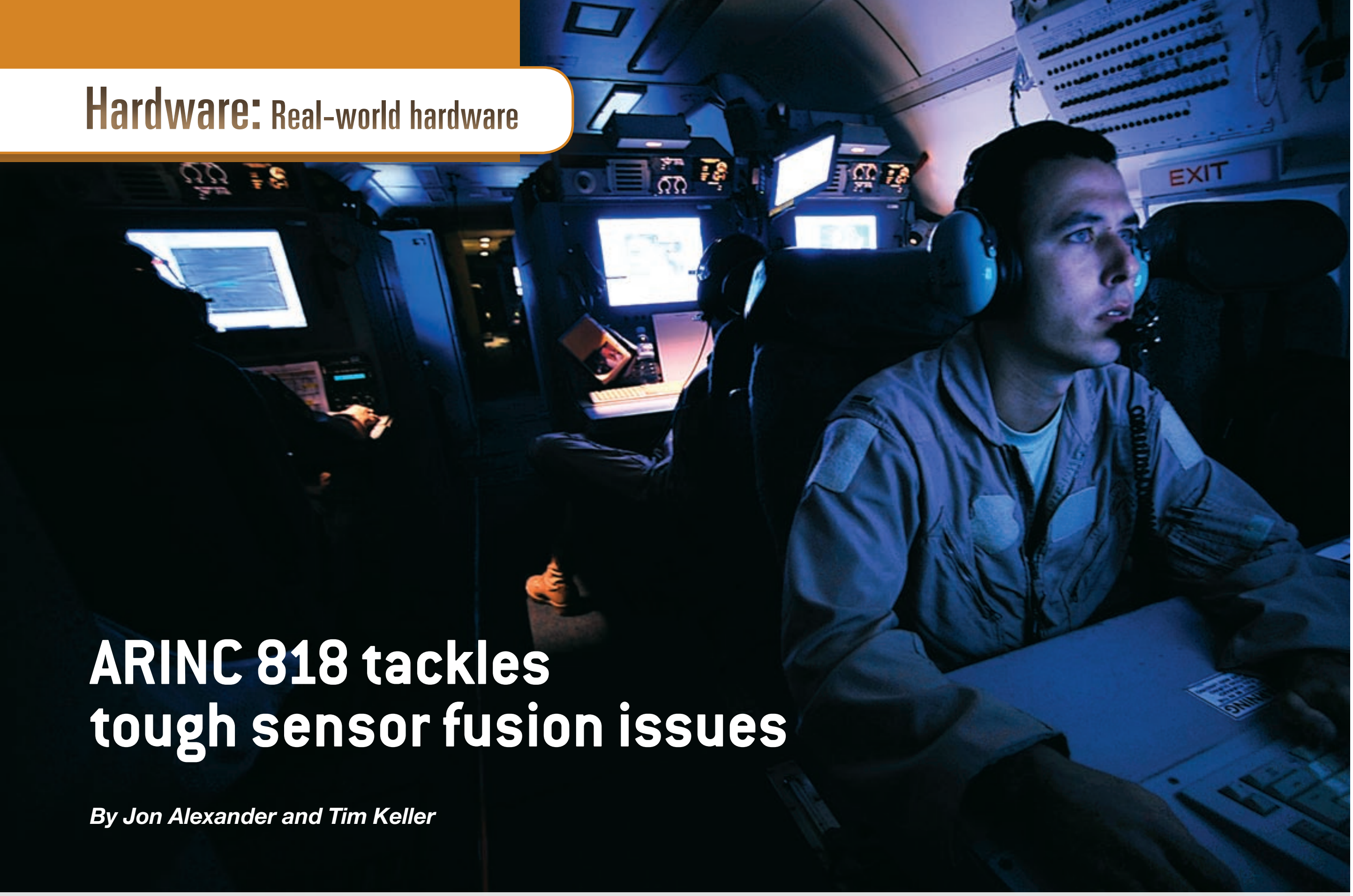
***Andy Finch** is a product manager for SprayCool. Since joining SprayCool in 2000, he has held engineering and management positions supporting program management, product development, and systems engineering. Prior to SprayCool, he developed control systems and automated equipment for the food processing, agricultural, and HVAC industries. Andy earned a BSME from the University of Idaho, an MS in Engineering from Purdue University, and an MBA from Indiana University. He can be contacted at afinch@spraycool.com.*

***Jeff Weiler** is a technical director for SprayCool. Since joining the company in 1992, he has held a variety of engineering and management positions, with responsibilities including technical oversight into product development, concept development, sales and business development, and customer interface. Jeff earned a BSME from Washington State University. He can be contacted at jweiler@spraycool.com.*

SprayCool
866-993-2665
www.spraycool.com



U.S. Air Force photo by Staff Sgt. Aaron Allmon II

ARINC 818 tackles tough sensor fusion issues

By Jon Alexander and Tim Keller

Sensor fusion systems continue to proliferate in military applications like surveillance, target tracking, and missile defense, but they bring their share of system-level challenges such as sensor synchronization, cabling weight, distance restrictions, and EMI. The authors discuss how ARINC 818 (Avionics Digital Video Bus) can be used as a flexible sensor interface to solve these system-level issues. Additionally, a bidirectional ARINC 818 system architecture scheme for time multiplexing multiple sensors onto a single fiber and implementing a return-path for sensor command and control is described.

As sensor fusion systems proliferate in applications like enhanced vision, surveillance, target tracking, and missile defense, many system-level challenges exist when processing is executed remotely from the sensor pod including: sensor synchronization, cabling weight, distance restrictions, and EMI. The ARINC 818 protocol, which has been used extensively in aerospace video systems such as cockpit displays, can be used as a flexible sensor interface to solve these system-level issues. A bidirectional ARINC 818 system architecture is described including a scheme for time multiplexing multiple sensors onto a single fiber and implementing a return path for sensor command and control.

Overview of ARINC 818 protocol

ARINC 818 is relatively new, and many engineers are not yet familiar with the protocol. Before describing how to use ARINC 818 in sensor fusion systems, an overview of the protocol will aid the discussion.

The standard, titled *Avionics Digital Video Bus* (ADVB), is based on the Fibre Channel Audio Video (FC-AV) standard and is an adaptation of Fibre Channel that adds video transport capabilities. But where the FC-AV standard intends to support a very broad set of industries and applications, ADVB focuses on the critical needs of avionics video. ADVB is simplified from FC-AV with no requirements for link initialization, flow control, or other Fibre Channel exchanges such as port login. ADVB is defined as a unidirectional link, and although simplified, ADVB retains attributes of Fibre Channel that are beneficial for mission-critical video applications, such as high speed, high reliability, low latency, and flexibility.

Additionally, ARINC 818 is a point-to-point, 8B/10B encoded protocol for serial transmission of video and data. The protocol is packetized, video-centric, and very flexible, supporting an array of complex video implementations including the multiplexing of several video streams onto a single link. ARINC 818 and FC-AV define link speeds from 1 Gbps to 8 Gbps with a bandwidth up to 800 MBps, which accommodates the most demanding sensor-fusion applications.

ADVB packet structure

The ADVB frame shown in Figure 1 is ARINC 818's basic transport mechanism. It is important to refer to these packets as "ADVB frames" rather than simply as "frames," to eliminate potential confusion with video frames.

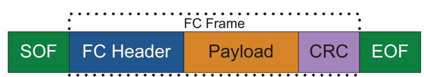


FIGURE 1: The ADVB frame is the basic transport mechanism for ARINC 818.

The start of an ADVB frame is signaled by a Start-Of-Frame (SOF) 4-byte ordered set and terminated with an End-Of-Frame (EOF) ordered set. Every ADVB frame has a standard Fibre Channel header comprised of six 32-bit words. These header words pertain to such things as ADVB frame origin and intended destination and ADVB frame position within the sequence. The Source ID (SID) field in the ADVB frame header allows video from each sensor to be distinguished from the other sensors.

The “payload” contains either video, video parameters, or ancillary data. The payload can vary in size but is limited to 2,112 bytes per ADVB frame. To ensure data integrity, all ADVB frames have a 32-bit Cyclic Redundancy Check (CRC) calculated for data between the SOF and the CRC word. The CRC is the same 32-bit polynomial calculation defined for Fibre Channel.

ADVB container structure

The ARINC 818 specification defines a “container” as a set of ADVB frames used to transport video. In other words, a video image and data are encapsulated into a “container” that spans many ADVB frames. The “payload” of each ADVB frame contains either data or video. Within a container, ARINC 818 defines “objects” that contain certain types of data. That is, certain ADVB frames within the container are part of an object. The four types of objects found within a container are shown in Table 1.

Object	Data
0	Ancillary data
1	Audio (not used)
2	Video: progressive or odd field
3	Video: even field

TABLE 1: ADVB frames within the container are part of an object, and four types of objects are found within a container.

In most cases, a single container maps exactly to a single video frame. An example will clarify how video is transported: To transport an XGA video frame (1,024 x 768, 24-bit color), ARINC 818 will use a total of 1,537 ADVB frames. The payload of the first ADVB frame holds container header information and ancillary data; this will be followed by 1,536 ADVB frames, where the payload of each ADVB frame holds half a line of video.

ARINC 818 sensor fusion interface architecture

Figure 2 shows an architecture for interfacing with three sensors. A sensor interface module, colocated with the sensors, is used to time multiplex video from three sensors onto a single ADVB link. In this example, there are two IR sensors, each with 14 bits per pixel and 640 x 512 resolution at 60 Hz and a 1,024 x 768, 24-bit color optical sensor. Together, these sensors require 220 MBps of throughput and can be multiplexed onto a single 3.1875 Gbps ARINC 818 link.

The architecture includes an ARINC 818 command and control path from the receiver. In the example, the command and control path is shown as ARINC 818, but it could be achieved with an RS-422 or similar data bus if a high-speed bus like ARINC 818 isn’t required. In this example, ARINC 818 (3.187 Gbps) is more than 300 times faster than RS-422 (10 Mbps).

The sensors may also have ARINC 818 interfaces. An ARINC 818 interface can be designed into the sensors using either a COTS converter board (for example, RS-170 to ARINC 818) or an ARINC 818 IP core implemented in an FPGA.

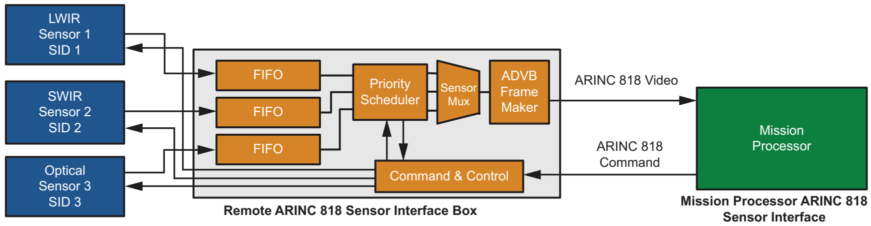


FIGURE 2: A sensor interface module, colocated with the sensors, is used to time multiplex video from three sensors onto a single ADVB link.

Time multiplexing video onto a single link

ARINC 818 is built on a networking protocol where packet header IDs allow for multiplexing multiple sensors onto a single fiber. Multiplexing onto a single fiber reduces the number of cables and connectors, reducing weight. The Source ID field in the ADVB header is used to distinguish video or data from the different sensors. In our example, SID=1 is an LW IR sensor, SID=2 is an SW IR sensor, and SID=3 is an optical sensor. Figure 3 shows how packetized video lines in the ADVB frames are interleaved on the link.

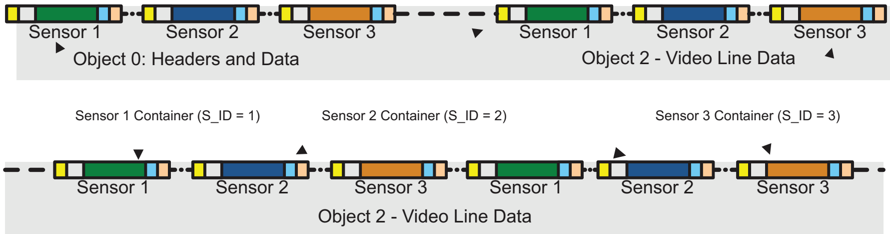


FIGURE 3: Packetized video lines in the ADVB frames are interleaved on a link.

Command and control interface

A primary focus of ARINC 818 is flight deck video connections, and the standard defines only a unidirectional link. However, a second link can be added in the reverse direction for command and control. As a command and control link, the ancillary data field in Object 0 is used for small data packets such as a sync pulse, whereas Objects 2 or 3 are used to send "image size" data such as bad pixel replacement maps or Non-Uniformity Correction (NUC) gain and offset values. The command and control link can have a faster or slower update rate than the video link.

Typical parameters to be sent over the command and control link may include: integration time, sync signals, NUC, sensor mode (standby, BIT, or normal), test pattern, bad pixel replacement, read temperature, pixel gain/offset data, and calibration and test pattern data. These parameters are the payload of the ADVB frames and are inserted into Objects 0, 2, or 3 on the command and control link depending on the type of data.

ARINC 818: Combating system-level issues

We will now examine the four system-level challenges alleviated by ARINC 818: video synchronization, along with weight, distance, and EMI.

Video synchronization

With the sensor pod located remotely from the fusion engine, the first step in complex image fusion processing requires time synchronization of images. Current approaches for this involve buffering several image frames from each sensor so that the image-processing algorithm can apply the right time offsets to the stored data. However, buffering several video frames creates a delay on the order of 16 ms to 48 ms that can be too much for tight-latency budgets of time-critical applications such as Head-Up Display (HUD) takeoff and landing assist.

In contrast, an ARINC 818 return link offers a way to genlock sensors so that the received image data will be very closely correlated in time. For example, the sensor interface block can use the arrival of the OBJ 0 frame as a genlock trigger for the sensors. This can be as simple as sending a genlock sync pulse upon detection of each SOFi. (A SOFi is the first SOF in a sequence.) But more likely, for enhanced vision applications using heterogeneous sensors with differing internal latencies (microseconds to milliseconds), the sensor interface box command and control will need to apply independent delays to the sensor triggers. Trigger delay values can be included in the ARINC 818 return link data, thereby allowing the receiver to directly control the skew between incoming sensor images. Trigger delays can be set during start-up calibration, or if needed, changed in real time. This system-level approach can allow for sensor images to be very closely correlated in time, eliminating the burden in the receiver for buffering several full images. More importantly, this approach reduces latency contribution from full-frame times (10s of milliseconds) to line time (100s of microseconds).

Weight, distance, and EMI

In addition to video synchronization, ARINC 818 also has many advantages in weight, distance, and EMI. First, an ARINC 818 fiber optic implementation significantly reduces weight for the system. For instance, if the sensor pod is located 15 meters from the image processing and typical copper interfaces are used, there will be three sets of coax cable carrying the video signals and three sets of twisted, shielded cable to carry a command and control signal such as RS-422. The cable weight of aerospace-grade coax is 15 g/m, and twisted, shielded is 20 g/m. The total cable weight will be 1,575 g. An ARINC 818 system will include a sensor interface box weighing 380 g and a dual-fiber cable weighing 15 g/m, for a total weight of 605 g yielding a 62 percent weight savings. (Connectors were not included in the calculations because there is such a wide variety of connectors that could be used.)

Since ARINC 818 uses either single-mode (up to 10 KM) or multimode (500 M) fiber, distance is typically not an issue. Compared to a 10 M limitation on CameraLink or 5 M on IEEE 1394 (Firewire) or DVI, even ARINC 818 over copper is superior, with distances of 25 M at 1 Gbps and 15 M at 2 Gbps. Most commercial and military aerospace applications use ARINC 818 over multimode fiber. The added advantage of fiber optic cabling is EMI immunity, which eliminates the need for shielding inherent in all copper cables Using fiber for high-frequency transmissions like ARINC 818 eliminates issues with both radiated emissions that interfere with other electronics and EMI susceptibility that degrades data integrity.

ARINC 818 benefits modern sensor fusion systems

In sensor fusion systems where sensors are located remotely from the sensor fusion engine, ARINC 818 offers advantages in synchronization, bandwidth, weight, distance, and EMI immunity. COTS components like interface converters and ARINC 818 IP cores facilitate implementing ARINC 818 in demanding sensor-fusion applications. For more information on ARINC 818, visit www.ARINC818.com.

***Jon Alexander** (MSEE) is senior engineer, CEO, and founder of Great River Technology, which specializes in high-performance digital video systems for aerospace and military customers. Jon has 20 years of experience in electronics design and served on the ARINC 818 standards committee. He has also been a chief designer of numerous ARINC 818, FC-AV, and HOTLink systems. He can be contacted at jalexand@greatrivertech.com.*

***Tim Keller** (MSEE) is director of product development at Great River Technology. He served on the ARINC 818 committee and drafted key specification sections. Prior to joining Great River Technology in 2005, Tim worked for 16 years as a control systems engineer for real-time embedded systems at Honeywell. He can be contacted at tkeller@greatrivertech.com.*

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Meeting the challenges of portable military devices with low-power design techniques

By Lee Brindel

U.S. Navy photo by Photographer's Mate 1st Class David C. Lloyd

Today's portable military devices have strict requirements when it comes to Size, Weight, and Power (SWaP), which can make designing a field-appropriate device very challenging. A successful low-power mil-spec design with extended runtime is possible; however, designers must focus on specific feature and component selection, utilize careful hardware management, and select power-efficient displays and software.

Size, Weight, and Power (SWaP) are the three most important elements in portable military device design. If the system is too bulky, it cannot be carried, and if it runs out of power, it cannot be used. A focus on power can help solve all three SWaP requirements, because the power needed directly impacts the size of the required batteries, and larger batteries compromise the size and weight constraints of portable devices. In order to design a successful portable device by maximizing power and minimizing size, electronics and applications must be designed for low power. The problem is that selection of some feature sets and components or even displays can significantly reduce battery life, as can running them on inefficient enabling software.

Accordingly, extending battery life begins with strategic selection of the feature set and components, followed by careful hardware management. Displays must be vigilantly researched and managed, as displays are often the most power-hungry feature of a portable device. However, displays have become crucial to successful military device design as evidenced by the increased popularity of touch screens in such devices. Effective software management should also be utilized to minimize power consumption (and thus device size) without compromising system performance.

Targeted feature and component selection

Careful selection of a feature set and components is required to maximize battery life while maintaining optimum functionality. When choosing a feature set or components, target only essential features, hence avoiding spending energy on unused components. Power consumption of common features is often underestimated, so it is important to understand the power impact of each major feature. For example, power consumption of some interfaces, such as UARTs and GPIOs, is negligible, while other interfaces such as cellular modems are capable of using up to 3 W. Unexpected power consumption can also occur with wired interfaces, which are generally assumed to be low power. For example, higher-speed wired interfaces, such as USB or Ethernet, can consume as much power as a wireless interface (Table 1). This power consumption is in addition to increased processor power to parse data from these devices.

Max power consumption of common interfaces	
Cellular modem	3 W
Wi-Fi modem	800 mW
Ethernet controller	400 mW
USB hub	800 mW
GPS receiver	200 mW
Bluetooth modem	300 mW

TABLE 1: Higher-speed wired interfaces, such as USB or Ethernet, can consume as much power as a wireless interface.

Managing the hardware

After establishing the appropriate feature set and selecting the necessary low-power components, managing hardware is the necessary next step in creating a military device that meets SWaP requirements. Power-saving techniques must be implemented to reduce the power of hardware when not in use, and thus reduce the need for a larger battery that could compromise the SWaP of a portable military device. The most common technique is using switchable voltage rails on unused hardware. The primary advantage of switching off voltage rails is that the hardware will use no power. This technique will offer best results when the device interconnection to the rest of the system is simple such as a USB port or UART. But designers should be aware that when powered-down hardware has I/O lines going to several powered system components, interference with the remainder of the system might occur as a result of these lines behaving unexpectedly. From this state, it is also quite possible that hardware might not re-initialize smoothly after being switched on again. Proper power sequencing and re-initialization of the disabled hardware must be executed to ensure that the device is again working properly.

Another power-saving hardware management technique is the proper use of low-power modes, including reduced functionality and sleep states. Unlike switchable voltage rails, the data lines will go to a safer high-impedance mode that will generally not interfere with overall system operation. Another advantage is that the device will typically recover more quickly than a switchable rail when resuming to full operation and will not require as much re-initialization. A device does still consume some power in sleep mode, but consumption is generally nominal. Some components offer limited functionality states where not every feature is available, or the capabilities are limited. For example, many processors have the ability to scale core frequency and voltage, which is called *Dynamic Voltage and Frequency Scaling* (DVFS). The processor is still running but at a reduced frequency and cannot process data as quickly. A combination of these hardware management techniques will substantially reduce the power consumption of a portable military device.

Selecting the right display

When it comes to balancing power budgets with performance, displays provide a unique challenge – particularly in military devices, where power and size requirements are among the strictest. Therefore, LCDs are typically not the best choice because mil-spec devices often require extended runtime, along with daylight readability as the devices are often used outdoors in direct sunlight for prolonged periods of time. Although the trend has been to increase display brightness, this greatly impacts devices' battery life, leading to a larger battery and device or to shorter runtime. To manage the balance between display usability and military requirements, a number of power-savvy display options are available. The most interesting and promising are emerging technologies such as Active Matrix Organic Light-Emitting Diodes (AMOLED) displays and Electrophoretic Displays (EPDs).

AMOLED displays (left, Figure 1) provide high-contrast, vivid colors, are viewable in sunlight, and do not require a backlight, unlike its LCD predecessor (right, Figure 1). Most of the power of an LCD is consumed driving the backlight, which must be on in order to view the display. In contrast, the organic material used in each cell of the AMOLED emits light when voltage is applied, hence AMOLEDs do not require a backlight. This greatly reduces the display's portion of power consumption in the device when displaying bright colors on only portions of the display. Another key aspect of AMOLEDs that makes them well-suited for mobile devices is their high contrast ratio, which is typically 10,000:1, whereas, LCD displays are typically on the order of 300:1 or 500:1. This high contrast ratio means that when comparing an AMOLED with an LCD of the same brightness, the AMOLED will be more daylight readable.

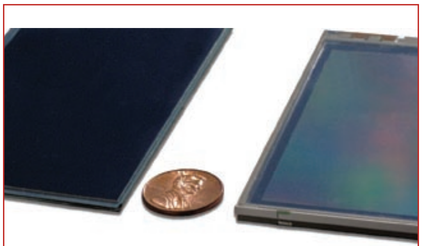


FIGURE 1: An AMOLED display (left) provides high-contrast, vivid colors, is viewable in sunlight, and does not require a backlight, unlike its LCD predecessor (right).

Even more power efficient than AMOLED displays are EPDs, or electronic paper. EPDs are a persistent, bi-stable display, meaning they only require power to update the image, not to maintain the image. EPDs have characteristics of paper and can be viewed in ambient lighting or with night-vision devices Commercially, EPDs can be found in products like Sony PRS readers or the Amazon Kindle. Militarily, the EPD can be found in rugged mil-spec devices such as the Soldier Flex Personal Digital Assistant (SFPDA), which was created by InHand Electronics in cooperation with Natick Soldier Research Development and Engineering Center and Army Research Lab, Sensors Electronic Device Directorate, and in collaboration with Artisent, Inc., E-Ink Corp., and the Flexible Display Center (FDC) at Arizona State University (ASU).

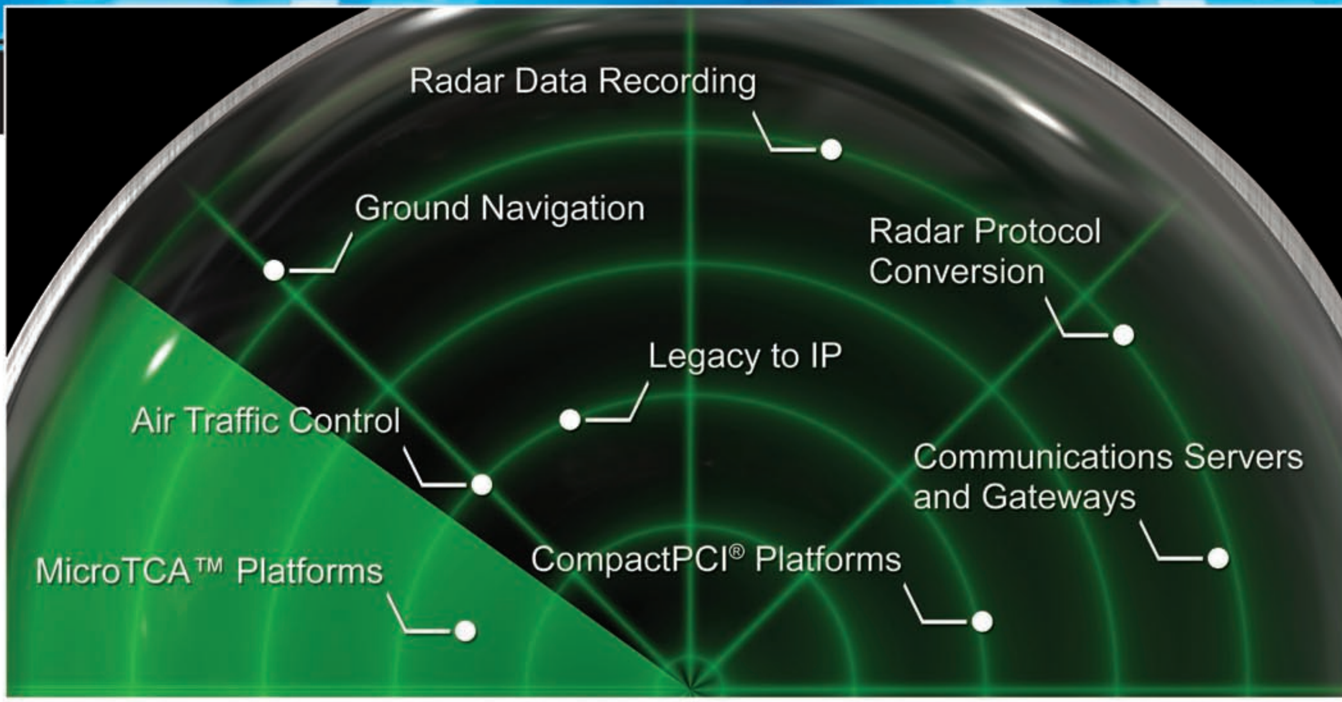
The SFPDA (Figure 2), designed for longer missions in the field, has a typical power consumption well under 1 W, including device display and a standard peripheral set. The SFPDA combines both low-power military handheld and flexible display technology. The SFPDA's reduced power consumption is due to EPD low-power characteristics, careful feature selection, and InHand's BatterySmart software, resulting in a ruggedized, mil-spec handheld providing more than six hours of continuous runtime and weighing less than one pound.

FIGURE 2: The SFPDA, designed for longer missions in the field, has a typical power consumption well under 1 W, including device display and a standard peripheral set.

Managing software

As mentioned in the SFPDA example, advanced runtime is pivotal in military devices, and software plays a large part in managing power consumption. Even with careful selection and management, it is possible to have a device capable of consuming 3 to 5 W in interfaces and display alone. Therefore, hardware usage must be carefully managed through software to ensure sufficient battery life while maintaining performance. Decreasing power consumption through well-written code is essential to increasing battery life and decreasing device size.

Software applications written for portable devices that make effective use of processors' Dynamic Voltage and Frequency Scaling (DVFS) will dramatically reduce power consumption. Ideally, the system processor should be fully powered only when needed, then turned back down when



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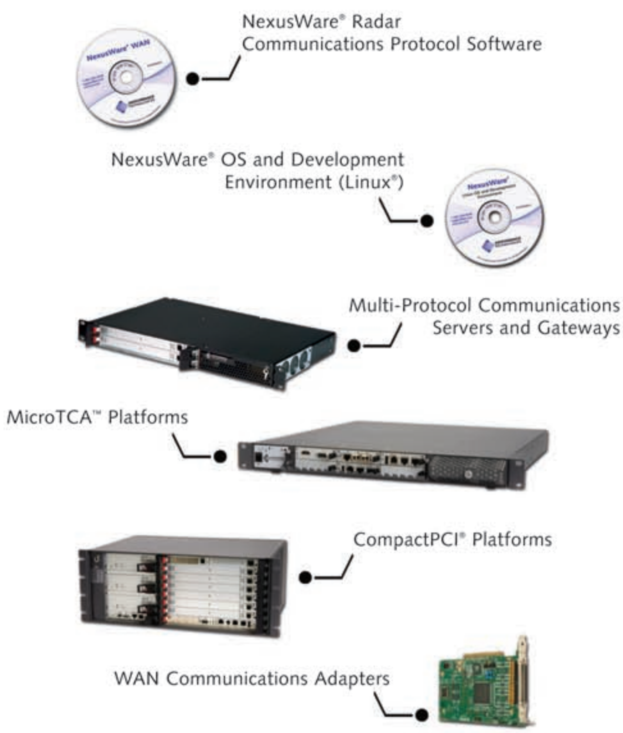

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the system is idle. Intense processing from video and communications does not allow processors' voltage and frequency to be manipulated without affecting performance. Strategies such as applications using interrupts instead of polling, using thread suspend states, and attempts to minimize communications will permit the processor to make the most of DVFS. When managing DVFS, a separate application will likely be required to prevent specific unit applications from fighting over the system processor's state. The example in Table 2 shows how much power can be saved by utilizing a power management suite. [The example in Table 2 uses InHand Electronics' BatterySmart software on a Fingertip4 (COTS PXA270 SBC) running WinCE, which shows more than 500mW of saved power with just the use of the BatterySmart suite.]

Meeting today's demand for low-power mil applications

Achieving the strict SWaP requirements of today's portable military devices truly centers around power consumption, as size and weight are dependent thereon. Accordingly, achieving low power consumption begins with feature set and component selections. To minimize power consumption, feature sets must be limited to only the necessities, while employing low-power hardware management. Often the largest component, displays can compromise system life and SWaP if not properly chosen. Thus, it is important to manage all aspects of the design – including utilizing power-efficient software. With proper software management, system power consumption can decrease up to 30 percent, which, in turn, will minimize size and weight. Ultimately, these tactics can help engineers successfully design a portable military device that meets all of its SWaP requirements.

InHand Fingertip4 52 MHz at 1,400 mV core voltage
(Evaluation of system in an idle state: includes a Fingertip4, daughtercard, LCD, and CF card)

Input voltage	5 V	9 V	14 V
Idle FT4, no power management	2.415 W	2.241 W	2.268 W
Idle FT4 with BatterySmart enabled	1.810 W	1.746 W	1.792 W

TABLE 2: An analysis of InHand Electronics' BatterySmart software on a Fingertip4 (COTS PXA270 SBC) running WinCE, showing more than 500 mW in saved power.

Lee Brindel *is a systems engineer at InHand Electronics, supporting the sales and marketing teams as the technical lead for embedded systems and managing customer requirements through the design process. Prior to InHand, he worked as a project engineer, focusing on utility power management. Lee holds a BSEE from Purdue University. He can be contacted at lbrindel@inhand.com.*

InHand Electronics
240-558-2014, ext. 227
www.inhand.com

MicroTCA's role expands in modern battlefields

By David Pursley

DoD photo by Lance Cpl. Kelsey J. Green, U.S. Marine Corps

Even against military embedded mainstays CompactPCI and VME and the up-and-coming VPX, MicroTCA is proving itself a powerful design option in harsh environments with: high bandwidth in a small form factor and proven ruggedness, multicore support, and high availability. Additionally, standards development is fueling MicroTCA's rapid movement as a military design choice from command centers to shelters to the battlefield.

Standardization initiatives throughout the military are driving integrated battlefield management, moving designers and technology evolution well past legacy architectures and toward more powerful yet standard solutions that can be deployed quickly and cost effectively. Military designers tend to need something deployable within a very well-defined timeframe and budget: Time and costs to modernize must remain under control, especially when contractors are used for developing designs that are then funded for production.

At the same time, high-tech military programs supporting network-centric operations such as Future Combat Systems (FCS), Joint Tactical Radio Systems (JTRS), and Warfighter Information Network-Tactical (WIN-T) are heavily communication-centric, requiring orders of magnitude more bandwidth than previous generation programs. Couple this with a growing demand for improvements in issues of Size, Weight, and Power (SWaP), and the military is fast driving toward smaller form factors offering portability and very high performance. With military design expertise deeply rooted in VME and CompactPCI, designers face new challenges in learning about the functional differences between these options – along with the much-newer contender VPX – versus MicroTCA. Today's MicroTCA is proving that it can meet the demands of the front lines, with its SWaP-savvy high bandwidth, military-proven ruggedness, as well as its multicore support and High Availability (HA).

Bandwidth mingled with SWaP: In context

VME and CompactPCI are 6U and 3U architectures that provide communication via a shared data bus. They provide enough bandwidth between master and slave devices (320 MBps for VME64) for many onboard vetronic, navtronic, and avionics applications, but newer programs require more bandwidth. Switched fabric extensions to these architectures (VITA 31, VITA 41, and PICMG 2.16) offer additional interfaces such as dual GbE to improve overall bandwidth, but they are only available in a 6U form factor, which can be prohibitive to smaller designs. Moreover, many of today's communications-centric military applications require even more bandwidth.

However, the MicroTCA standard has risen to address the issue of meeting both SWaP and bandwidth requirements. MicroTCA was ratified in July 2006 as PICMG MTCA.0. (See sidebar on MicroTCA standards update.) MicroTCA is defined by the high processing capacity and extremely high communication bandwidth it brings to a small 2U form factor. When compared with 6U, MicroTCA achieves greater bandwidth in smaller spaces, meeting the growing need for SWaP considerations in high-end military designs. MicroTCA offers up to 21 high-speed serial connections on the backplane – versus the two generally found in VME and CompactPCI implementations – each giving up to 2.5 Gbps bandwidth.

Additionally, MicroTCA delivers more communication bandwidth and higher computational abilities using multiple processors on a single backplane. 6U VME or CompactPCI designs can deliver this too, but necessary form factor adjustments to 3U limit the bandwidth compared to MicroTCA. MicroTCA falls at the large end of the small form factor universe, but at 2U x 3-6HP x 183.5 mm, it is a smaller form factor than even 3U VME and Compact PCI.

The rugged decision: VPX or MicroTCA?

When considering MicroTCA, designers could also explore VITA 46, known as the *VPX* architecture. Mission-critical applications functioning in very rugged environments – such as conduction-cooled ground mobile installations – are ideal for the uniquely rugged processing power of VPX. Specifically targeted to high-end, ultra-rugged military applications, VPX technology tends to be expensive. As a result, MicroTCA meets the design cost parameters of a greater group of applications, and is well suited to moderately rugged applications.

Rugged MicroTCA standards update

Standard COTS MicroTCA systems are more than rugged enough for environments such as ground installations or on airborne platforms. MicroTCA boards and systems are designed to meet NEBS Level 3, which includes requirements such as thermal margins, fire suppression, emissions, and the ability to remain operational during a severe earthquake. But further ruggedization of MicroTCA holds significant interest for the mil/aero design community – and it's coming.

A working group of the PICMG standards body is driving standardized rugged implementations of MicroTCA, including rugged air-cooled MicroTCA (MTCA.1 and MTCA.2) and conduction-cooled MicroTCA (MTCA.3). These efforts are leveraging work done in the ANSI/VITA 47 specification to define the environments in which the boards will perform.

The first of these MicroTCA specifications, MTCA.1, is currently under draft review for ratification. MTCA.2 extends MTCA.1 into more rugged military environments such as those defined by ANSI/VITA 47's EAC6 environmental class and V2 vibration class. Meanwhile, the MTCA.3 specification defines a conduction-cooled interface that allows AdvancedMCs to meet the thermal, shock, and vibration profiles defined in ANSI/VITA 47: temperature ranges of -40 °C to +85 °C at the card edge, 40 *g*, 11 ms operational/operating shock, and random vibration profile suitable for rugged ground mobile applications.

Additionally, MTCA.3 will address systems that are conduction cooled with no airflow in sealed environments. MCTA.3 is underway with PICMG, and designers can anticipate that this will pit VPX against MicroTCA as competing design options. Initial testing has been promising, and rugged MicroTCA options are already available and being deployed in advance of these standards.

Accordingly, when considering whether a new project should utilize VPX or MicroTCA, architectural choice is vital (Table 1). At a very basic level, MicroTCA and VPX are targeting the same problem for the military but from two completely different perspectives: VPX is extremely rugged and currently has no real path to a less costly, more widely applicable solution. MicroTCA by contrast is starting out as a less-rugged, lower-cost solution, but is now specializing its rugged features through follow-on specs designed for specific rugged elements. However, both form factors have their place.

If development time is slightly less of a factor – say, for an application being deployed sometime next year – and if the application is running in a ground vehicle rather than an aircraft, VPX could be an excellent design choice for its ruggedness. If the application in question is running on a jet or fighter plane, a platform such as MicroTCA – proven both in terms of communication bandwidth and ruggedness – could be the best design choice.

Hence, MicroTCA is being used in more rugged applications these days. In fact, BAE Systems has conducted tests that reveal that MicroTCA is rugged enough for even ground mobile applications (Figure 1). In this testing, they found that the MicroTCA edge connector was sufficient for vibration profiles necessary for the WIN-T JC4ISR radio. Specifically, testing showed that there were no discontinuities and that the contacts did not abrade after the equivalent of a 25-year life cycle.

FIGURE 1: MicroTCA is proven rugged enough for even ground mobile applications.

	CompactPCI	VME	PICMG 2.16	VPX	MicroTCA
Form factor	3U x 160 mm	6U x 160 mm	6U x 160 mm	3U x 160 mm	73.5 mm x 181.5 mm
CPU to CPU communication	1 CPU board typical	VMEbus	GbE	GbE, 10 GbE	GbE, 10 GbE
Peripheral communication	PCI Bus	VMEbus	PCI Bus	PCI Express, Serial Rapid IO	PCI Express, Serial RapidIO
Hot swap of line cards	Peripherals only	No	Yes	No	Yes
Rugged	Yes	Yes	Yes	Yes	Underway
Widely applicable	Yes	Yes	Yes	Military-centric	Yes

TABLE 1: When considering whether a new project should utilize VPX, MicroTCA, or another form factor, architectural choice is vital.

Multicore and high availability: Mission critical

MicroTCA's high bandwidth for both communications and computing can accommodate 12 compute blades on a single backplane. Now imagine that same 2U system, but with those 12 blades each utilizing a multicore processor. If that becomes a 3U or even 4U system, it could have as many as 24 cores today. That would be achieved in a very small footprint, which is perhaps the most unique advantage of MicroTCA. In addition, communication bandwidth capabilities range from 40 Gbps to >1 Tbps. This wide range is realistic because actual bandwidth will depend on the implementation. Meanwhile, typical PICMG 2.16 or VITA 31 applications offer 2 Gbps.

In addition to its expansive multicore computing capabilities, MicroTCA also provides high-availability capabilities. High availability was not always a requirement for earlier military systems, but that is changing as integrated battlefield management demands maximum system uptime. Monitoring the health of a system and then "healing" it in the field is a plus with MicroTCA. (MicroTCA and AdvancedTCA were built with HA in mind, which means that HA doesn't add much to the cost because the infrastructure already supports it.) Through an Intelligent Platform Management Interface (IPMI), users can be notified when the system is not running at peak performance. Fans can be turned on and off automatically as temperature thresholds change, and if a board fails, it can be removed and replaced with the system up and running. IPMI-based health monitoring, along with full redundancy with fail-over, prevents any single point of failure in the system.

MicroTCA in today's battlefield

Modern military systems require high computing and communications bandwidth to link soldiers to vehicles, aircraft, ships, and command centers. These complex systems also require greater communication bandwidth and smaller footprints, which means that high-end processing in small form factors is a key design element moving forward. Designers of modern warfare systems must consider choices beyond traditional VME and CompactPCI architectures, recognizing where these legacy platforms fit and where other newer form factors such as VPX or MicroTCA hold the most promise for their rugged military system design. Multicore support and high availability are also important considerations when planning for today's battlefield technology.

__David Pursley__ is a field applications engineer with Kontron. He is responsible for business development of Kontron's MicroTCA, AdvancedTCA, CompactPCI, and ThinkIO product lines in North America and is based in Pittsburgh, PA. Previously, he held various positions as a field applications engineer, technical marketing engineer, and marketing manager. David holds a Bachelor of Science in Computer Science and Engineering from Bucknell University and a Master's degree in Electrical and Computer Engineering from Carnegie Mellon University. He can be contacted at david.pursley@us.kontron.com.

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Editor's Choice Products

Really rugged Pentium M 'shoebox' for kicks

With DoD budgets sure to be adjusted as President Obama changes U.S. foreign policy, the demand for low-cost yet rugged electronics is bound to accelerate. ADLINK is betting heavily on this trend, using their Ampro group to design mil-style industrial PCs that can go the distance. The company's 8" x 10" x 3" MilSystem 800 uses the shipboard-deployed RuffSystem 800 with uprating, derating, and ruggedizing tricks pulled right from the conduction-cooled board market. This 1.4 GHz Pentium M system boasts 1 GB of DDR memory, optional 32 GB of SSD, and up to 16 GB of rugged CF, or an HDD.

I/O comes out the front in the form of 38999-style military connectors, fed by 10/100/1000 Ethernet, four USB 2.0 ports, four serial ports, audio/video, PS/2, IDE, SATA, and an additional 55 user-defined I/O signals. But the core of this system is its rugged cost effectiveness. Designed to operate over -40 °C to +75 °C, the system uses a derated and guard-banded PSU, soldered CPU and Northbridge, thicker 0.093" PWB, and is backed by 901, 810, and HALT testing to *prove* survivability on the battlefield. This is one shoebox that can get kicked around.

ADLINK Technology • www.adlinktech.com • RSC# 41449

Low power Core 2 Duo rugged 'shoebox'

As the image shows, the PIP22 from MPL AG is made in Switzerland – and has just about as many features as the famous army knife. Designed for rugged industrial applications, the PC product relies on a Core 2 Duo L7400 off of Intel's rugged roadmap in order to promise a minimum five-year product life cycle. Operating from -40 °C to +65 °C, the fanless design is impressive in that it requires no CPU derating but still consumes a mere 30 W, fed from a range of 8-28 VDC (optionally 18-48 VDC). The case size is 270 mm x 162 mm, with heights ranging from 62, 83, or 120 mm depending upon internal options.

Promising a high MTBF due to mostly soldered components, the PIP22 can accommodate up to 3 GB of DRAM (1 GB soldered) but comes equipped with graphics (via Intel's 945GME), dual 10/100/1000 Ethernet, FireWire 800, USB 2.0, and RS-232/422/485 (two plus two optional). The unit talks to a variety of HDDs via one EIDE and two SATA ports; it also includes the standard PC/2, parallel, and even a legacy bootable floppy port. Best of all for defense applications, the shoebox is internally expandable via optional modules on PCIe minicard, PC/104-*Plus*, PMC, or PCI. Finally, really rugged specs are achieved via EMC (EN 55022, EN 55024, EN 61000, and MIL-STD-461E) and shock and vibration (EN 60068). Here's another shoebox ready to be kicked around.

MPL AG Elektronik-Unternehmen • www.mpl.ch • RSC# 41454

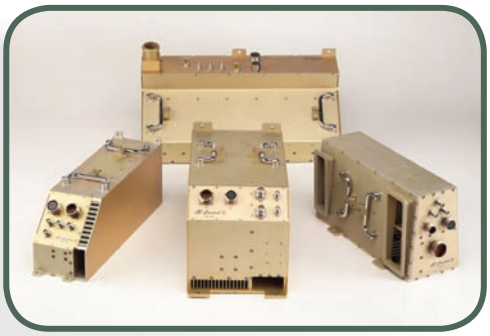
High-voltage aircraft DC-DC converters

Those of us in the digital realm are used to sub-5 VDC voltages … and occasionally we can think in terms of 28 VDC in vetronics applications. But avionics guys and gals dream of bigger numbers: on the order of 270 VDC. Higher voltages mean lower currents and smaller diameter wires (but with fancier dielectric insulation, to be sure). Running these kinds of voltages around airframes requires up- and down-converters at equipment nodes. Vicor's MIL-COTS Bus Converter Modules are designed to do just that, at efficiencies exceeding 95 percent.

The VMB0004MFJ (J-lead) and VMB0004MFT (through-hole) are designed to work with the company's 28 VDC PRM interface device to power loads operating from 1-50 VDC. Accepting inputs from 240-330 VDC, the BCM spits out an unregulated secondary voltage of 30-41.25 V at a nominal 235 W. The 95 percent efficient Sine Amplitude Converter (SAC) boasts an astounding 829 W/in^3 and Vicor claims a system footprint reduction of more than 40 percent. Built-in undervoltage, overvoltage lockout, overcurrent protection, short circuit protection, and overtemperature protection make at-the-node voltage conversion much easier and safer. Priced at around $105 in OEM quantities, avionics voltages might be complex, but designing the power conversion nodes doesn't need to be.

Vicor VI Chip • www.vicorpower.com • RSC# 41455

High-power airborne ECM microwave transmitters



Since we seem to be on an avionics kick this month, here's another airborne product set worthy of distinction: dB Control's Electronic Countermeasure (ECM) Microwave Power Modules (MPMs). This family of four MPMs provides up to a whopping 1,500 W in Continuous Wave (CW) or pulsed varieties. The RAM- or ECS air-cooled transmitters are conduction cooled and designed for extremely rugged environments while providing high reliability and EMI compliance to MIL-STD-461E.

Available in four flavors, the LRU-style MPMs are modularly designed to meet off-the-shelf and custom requirements: High-band transmitter, 6-18 GHz with 1,500 W at 5 percent duty cycle; high-band CW transmitter, 6-18 GHz with 100 W CW pulse; dual high-band transmitter, 6.5-18 GHz, 200 W per channel CW or pulse; and single low-band transmitter, 2-7 GHz, 200 W CW or pulse. All use highly efficient, mini-helix Traveling Wave Tube (TWT) technology with a low-noise, solid-state driver amplifier. They're also extremely compact and offer flexible packages for easy customization.

dB Control • www.dbcontrol.com • RSC# 41456

Rugged PDA with GPS, camera, altimeter

We city wimps whine when we miss an off-ramp or if the 12 V connector dislodges from our suction-cup-mounted GPS nav unit. But what do soldiers and Marines do when they're humping through the mountains and need a sit rep? They just might pull a GETAC PS535F rugged PDA from their rucksack. This handheld is not only a useful computer, but it also contains a 3 megapixel autofocus camera, altimeter, and E-compass.

The sunlight-readable 3.5" VGA touch screen is useful for moving maps, waypoints, or other Windows Mobile 6.1 software apps. Powered by a 533 MHz Samsung 2450 CPU with 128 Mb of MDDR and 2 GB of NAND flash, the unit can last up to eight hours on a battery charge. The altimeter and E-compass functions provide advanced navigation including longitude, latitude, and altitude, and the unit can connect to GIS servers or military databases via Bluetooth modem or mobile phone. Wi-Fi (802.11b/g) can be used when up-/down-loading collected telemetry or images. The PS535F weighs only 10.6 oz.

GETAC, a subsidiary of MiTAC Technology Corporation • www.getac.com • RSC# 41503

VME SBC does DSP, XMC, and graphics

If vendors like GE Fanuc Intelligent Platforms are going to introduce VME boards like the V8775, they're going to follow the desktop PC trend: Intel Core 2 Duo CPUs and lots of I/O. GE's new SBC is no exception. It uses Intel's 2.53 GHz T9400 mobile CPU with 6 MB of L2 cache, backed up by 4 GB of DDR3 SDRAM and a x16 PCIe interface with the GM45 chipset. This CPU is noted for its ability to execute decent DSP math computation, and the super large memory makes matrix operations possible. But this is a VME board, and the VME ecosystem hasn't been ignored in favor of desktop-like I/O.

For instance, there's a VXS (VITA 41.3) GbE option, and the onboard twin GbE ports are routed to the front panel. Also included are dual SATA, four USB 2.0, and two serial ports. The board includes one PMC/XMC site, but an optional mezzanine board adds three more. An optional ATI Radeon E2400 GPU provides another x16 PCIe, 1,920 x 1,080 resolution, and full HD HDMI. Designers can eschew the optional VXS and onboard PMC/XMC in favor of an eSATA port, one USB 2.0, and two more GbE ports.

GE Fanuc Intelligent Platforms • www.gefanuc.com • RSC# 41504

Continued on page 43

At VersaLogic we know about building dependable, high reliability embedded computers for mission critical applications. Our products have been designed into some of the most sophisticated and high profile military and aerospace equipment used today. Every board we make is ran through exhaustive inspections and quality tests, ensuring that we deliver only the best. And with our world-class service and five year availability guarantee, we'll always be there when you need us. Whether you need one of our standard products or a customized version, our skilled technical staff will work with you to meet your exact requirements. So before your program launches, choose the company with the quality and service to take you where you need to go.

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1.800.824.3163
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VERSALOGIC CORPORATION

Atom-based COM Express board for low-power handhelds

PICMG's COM Express form factor puts the CPU subsystem on the mezzanine and the system-specific I/O on the carrier card. This approach keeps the portion of the system that changes most with the market – the CPU – on a life-cycle upgradeable COTS daughtercard. American Portwell's PCOM-B214VG Type II COM Express board uses Intel's latest 1.8 GHz N270 Atom processor and up to 2 GB of single channel DDR2 SDRAM in a small form factor that measures a mere 125 mm x 95 mm (L x W).

The board uses industry standard 200-pin SODIMM memory, 945GSE and ICH7-M chipsets, and consumes only 10 W in fanless, portable military designs. I/O includes EIDE (with Ultra DMA 100/66/33), two SATA ports, three x1 PCIe, four PCI, and AC97 for high-def audio, along with eight USB ports and one for GbE. Graphics support via the Intel chipset is 2,048 x 1,536 at 85 Hz driving CRT, LVDS, TV-out, and SDVO.

American Portwell • www.portwell.com • RSC# 41505

Static source code analysis for C# and .NET assists with quality, security

You may have noticed a growing number of embedded PCs in defense applications. (Just look at any small form factor product.) Increasingly, these devices run a variation of Windows because deployed applications can be easily ported from the lab to the field within the Windows framework. Another trend is that some enterprise-like applications will use Microsoft's Visual Studio 2008 and the C# programming language. Thus, Klocwork, a company known for automated source code analysis tools, has recently added C# static source code analysis to Klocwork Insight as a means of finding critical bugs in C# code, including resource management and runtime failure errors.

Used with both C# and .NET, Insight's capabilities work with Microsoft Visual Studio 2008 to allow analysis at the earliest point in the development cycle: before code check-in. Out-of-the-box checkers include Invalid Object References, Incorrect Contractual Obligations, NULL Object Dereferences, Invalid Cast Operators, and Reverse NULL Object Deferences. Custom C# checkers can also be created through Klocwork's Checker Studio, an extensible GUI-based environment. The company's Insight tool also supports C, C++, and Java. The tool is useful for quality and security purposes. For example, security specialists can push security and architectural policies out to developers' desktops.

Klocwork • www.klocwork.com • RSC# 36761

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by the existing VSO VPX dot specs. VITA is trying to capitalize on the groundswell of VPX activity by endorsing Mercury's fast-track approach. And vendors like CWCEC (and their customers) are crying "foul" because they're purposefully being excluded from what is supposed to be a fair and "open" process. I think that everyone is *individually* right on this one – adding up to one big controversy that you'll hear more about in weeks to come.

That was then, this is now

Clearly, ultra-recent events denote that these controversial issues must be weighing heavily on Mercury, their OpenVPX partners, and many of the end-user primes who are supporting the OpenVPX concept: The week *Military Embedded Systems* shipped to printer, a press conference was held to announce the opening up of the OpenVPX Industry Working Group to all VITA members in good standing. Specifically, companies such as CWCEC, TekMicro Systems, and any other interested VPX supporter can now join.

The group will hold a two-day gathering (March 16-17) preceding the next VSO meeting in Orlando on March 18-19. Following confab on the newly established OpenVPX Steering and Working Group procedures, new members will also need to sign a memorandum of understanding and possibly pay a small administrative fee to cover overhead. Since Mercury assures me that OpenVPX is trying to mirror VSO's procedures, it should be straightforward to take the group's documentation back into VSO within six months. As well, the OpenVPX Industry Working Group isn't specifically worrying about Ex Ante and ITAR issues – but is certainly cognizant of the law since VSO will overlay its own bureaucracy onto the documents once back in VSO.

So I'm heartened that at the 11th hour, Mercury and its partners are putting the "open" spirit into OpenVPX by allowing any company to join. This certainly is consistent with one of their stated goals toward interoperability. In fact, Bob Ford, a Boeing representative familiar with OpenVPX, told me that interoperability between vendors will "reduce the market fragmentation in the types of [VPX] cards." Getting companies like CWCEC involved is the *only way that can realistically happen.*

Still, I'm troubled by the timing of all of this. Although Mercury and Friends have ultimately relented by allowing newcomers to join, the fact is that this effort was going on within Mercury from October 2008 until January 2009 when other companies quietly signed up. And another two months have passed before more companies could enter the group. Will they really have a chance to alter six months of nonpublic momentum? I suspect not, and more controversy will be brewing when the reality of forced board redesigns by non-OpenVPX vendors sinks in.

Chris A. Ciufo
Group Editorial Director
cciufo@opensystemsmedia.com

***Note:** Though as we went to press, the OpenVPX Industry Working Group announced that all interested VITA members could join, that still doesn't resolve the controversy of those 20 dot specs in VITA … and what's to become of them. Check out the April issue of* VME and Critical Systems *for our first Q&A with Mercury.*

OpenVPX Industry Working Group:
Open for business, or just controversy?

By Chris A. Ciufo, Editor

***Important editor's note:** OpenSystems Media, publisher of* Military Embedded Systems, *has relationships with many of the companies mentioned in this column. Some of these companies are advertisers or partners, and others – such as VITA Executive Director Ray Alderman – are regular article contributors to this magazine or its sister magazine* VME and Critical Systems. *It's important for you to be aware of these relationships, which might affect my "objective impartiality," even though I've done my best to represent all sides accurately and factually.*
Chris A. Ciufo.

We've been here before. About five years ago, VITA (formerly the VMEbus International Trade Association) announced a roadmap for the future, and its VPX (VITA 46) specification was clearly identified as the next-generation version of the venerable VME64 bus. Sure, there was some confusion over the VXS (VITA 41) specification versus VME, but the key distinction was that in order to switch your system to VPX you needed an entirely new and different backplane. VME, you might recall, is the number one open standard, COTS embedded board form factor used in harsh environment, deployed defense systems. VME is used in everything from missiles and large torpedoes, to avionics, ships, armored vehicles, and spacecraft. In a nutshell: What happens in the VME ecosystem is *hugely important* to the defense industry.

The background

The not-really-open OpenVPX Industry Working Group (www.mc.com/openvpx) was recently started by Mercury Computer Systems to essentially create the system-level specification for VPX that they hope will become the next generation of VME. But wasn't that what VITA's own efforts were supposed to create? What has VITA's Standards Organization (VSO) been doing all these years? And wasn't Mercury one of the two leading proponents of VPX? (The other one is Curtiss-Wright Controls Embedded Computing or "CWCEC.") If you're confused already, it's going to get worse as I peel away the layers for you.

You see, VSO has announced about *20* different "dot specs" ranging from ANSI/VITA 46.0 "VPX: Base Specification" to the brand new VITA 46.21 (covering a distributed switch architecture). After all these years of work and what might be a million man hours by dozens of companies, why would Mercury suddenly decide to work outside of the VSO to create what looks like an entirely new next-generation VME? Is this a brilliant marketing feint to bifurcate the market? Are they so angry at the VSO that they've decided to start their own standards organization? Many VSO member companies and military primes counting on the VSO version of VPX are asking the same questions. Programs specifying VPX include several subsystems in the Army's Future Combat Systems, the Marine Corps' G/ATOR, and the counter-IED program JCREW.

Much has been written about this Mercury versus VSO situation in the past several weeks. My esteemed journalist colleagues at *Military & Aerospace Electronics,* John McHale and John Keller, have both weighed in on this subject. In my extensive interviews and research, I've determined that Mercury – and presumably their partners including Aitech, Boeing, GE Fanuc Intelligent Platforms, Hybricon, Tracewell, and others – sees three deficiencies with the VSO's version of VPX:

- The lack of backplane interoperability between board-level vendors
- The lack of a cohesive system architecture versus a series of board-level subsystem architectures (and the lack of data/control/management/user plane features)
- How long it's taking VSO to move from Working Group specs to Released ANSI/VITA specs while vendors need to build and ship "ratified" hardware

Citing the PCI Industrial Computer Manufacturers Group's AdvancedTCA specification set (PICMG 3.0) as the right way to leverage COTS into defense, the Industry Working Group wants to sort these issues out and present back to VSO a *revised VPX system document* within six months. Ironically, VITA's own management supports this unorthodox vote of "no confidence" in VSO's Standard Operating Procedure (SOP). VITA Executive Director Ray Alderman told me that while "a lot of good work" was put into characterizing the bottom-up (board-focused) VPX architecture, "that activity hasn't captured the computer science of the *system* itself," and the non-VSO efforts represent a "unified approach." Yikes: Sounds to me like he's saying GM spent too much time designing nuts and bolts instead of cars. Alderman asserts that PICMG's own AMC specs were created by an outside group with Intel, then later spun into PICMG and fast-tracked to become a standard.

For their part, Curtiss-Wright Controls Embedded Computing is greatly concerned, as the company is hands-down the leader in VPX and has doubtless invested millions of dollars in designing VPX boards, backplanes, and systems. Worse, Mercury's "open" Working Group won't disclose any details about their version of VPX and they won't let CWCEC join the party until sometime in March 2009 when "all will be revealed." Does this merely give Mercury and Friends time to sort out their specs without worrying about naysayers and arguments – or time to create a system that nicely excludes CWCEC? And how can all of this possibly be condoned by VITA while leaving its own largest VPX supporter – CWCEC – out in the cold?

On the surface, everyone's motives seem pure. The OpenVPX Industry Working Group is trying to solve some legitimate technical issues that are not well defined

Continued on page 44

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Barriers were made to be broken.

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As a global leader in mil/aero electronics, GE Fanuc Intelligent Platforms has been, and continues to be, on the leading edge of technology. One customer describes our products as, "the most technically astute, reliable, and competitive among their peers." The same engineer calls them "innovative," "intelligent," "versatile" and "intuitive."

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FANUC

MIL/COTS DIGEST

The Defense Electronic Product Source

March/April 2009

In This Issue

Rugged can be small: from boards to "shoeboxes"

If the March Embedded Systems Conference is anything like last year, odds are there will be loads of Small Form Factor (SFF) boards and systems. In defense – where applications range from benign shipboard fire control, to desert-deployable tactical operations centers, all the way to space-borne payload controllers – SFFs are fast becoming the dominant COTS system.

In the following special *MIL/COTS DIGEST* on "Rugged Small Form Factors," you'll find a range of products from prepackaged shoebox systems complete with 38999-style connectors, to open-standard form factors such as PC/104-*Plus*, COM Express, EPIC, and others. As well, many of these boards are essentially PCs, so desktop software and tools are especially important to rugged SFFs. Accordingly, we've chosen a collection of software products for you. Finally, many rugged SFFs can be found in nondefense industries including industrial control, transportation, and automotive, so we've added a handful of products (and even a tester) from those industries.

And in this special issue of *MIL/COTS DIGEST,* compiled in conjuction with our sister publication *PC/104 and Small Form Factors,* contributing editor Don Dingee has written several interesting system-level SFF articles. In his article "Rugged SFFs for vehicles" on page 6, Don examines SFFs used in all kinds of "vehicles," such as automobiles, airplanes, and even UAVs. His point: "While we often think of rugged boxes as big, armor-plated behemoths [there is a] range of innovative technologies being designed into SFF platforms."

Chris A. Ciufo, Editor

Dual-core mission computer

The DuraCOR 810-Duo from Parvus Corporation is a rugged dual-core mission processor subsystem targeted for harsh military and homeland security C4ISR deployments. Measuring 10.60" (L) x 5.30" (W) x 5.30" (H) (269.24 mm x 134.62 mm x 134.62 mm), the platform has a PC/104 card cage with up to six spare slots for PCI-104 or PC/104-*Plus* expansion. Based on an open architecture COTS design with a low-power 1.5 GHz Intel Core 2 Duo processor, the DuraCOR 810-Duo is designed for compliance with MIL-STD-810F, MIL-STD-461E, MIL-STD-704E, and MIL-STD-1275D. The watertight vehicle-mount computer comes with a 79-pin MIL-C-38999 connector, vehicle-grade DC/DC converter, and integrated EMI/EMC filtering. Connectivity includes GbE and Fast Ethernet, six USB ports, two RS-232 serial ports, and LCD/VGA dual video display.

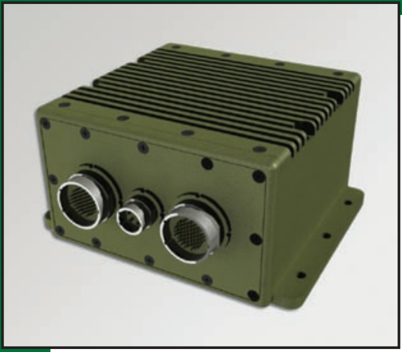
www.parvus.com **PARVUS CORPORATION**

Fanless PC/104 SBC

The Diamond Systems Helios is a ruggedized, compact, low-power, and low-cost PC/104 SBC. Helios utilizes the DMP Vortex86SX/DX single-chip processor operating at up to 800 MHz and has up to 256 MB of DRAM soldered onboard. The board offers standard PC peripheral features, including four USB 2.0 ports, one 10/100BASE-T Ethernet interface, four RS-232 ports (two with RS-232/422/485 capability), an IDE interface, and VGA/LCD graphics. It operates fanless over a -40 °C to +85 °C extended temperature range. Optional onboard data acquisition circuitry includes 16 16-bit analog inputs, four 12-bit analog outputs, up to 40 digital I/O lines, a 512-sample FIFO, and two counter/timers.

www.diamondsystems.com **DIAMOND SYSTEMS**

Rugged SFF PC



CodaOctopus Colmek's Stinger 553 is a rugged, tactical, small form factor PC built to MIL-STD-810F and MIL-STD-461E environmental standards as well as MIL-STD-704E power supply voltage standards, making it suitable for both military and civil applications. Designed to comply with IP65 and NEMA 4, its rugged aluminum chassis is built to take on harsh environments while operating over a temperature range of -40 °C to +85 °C. With an Intel Atom Z510/Z530 processor plus 2 GB of SDRAM and 4 GB solid-state disk onboard, the 5" x 5" x 3" (127 mm x 127 mm x 76.2 mm) unit can handle heavy computing loads.

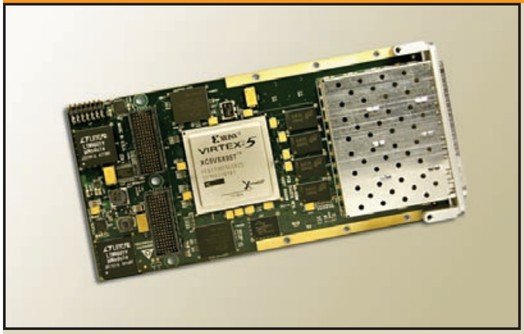
www.colmek.com **CodaOctopus COLMEK**

Atom-powered COM Express

The Toradex Woodpecker Z530 is a micro COM Express board based on the Intel Atom Z530 1.6 GHz processor with 533 MHz Front Side Bus (FSB). Compatible with COM Express Pinout Type 2, this 3.74" x 3.74" (95 mm x 95 mm) module includes 32 KB instruction cache, 24 KB L1 cache, and 512 KB L2 cache plus a SODIMM connector for up to 2 GB of DDR2 533 memory. In addition to an integrated Intel graphics video controller, the Woodpecker Z530 offers two PCI Express x1 lanes, a PCI interface, up to six Hi-Speed USB ports, a master and slave PATA interface, and two SATA interfaces. A 30-pin FFC connector provides two additional SDIO channels for Bluetooth and IrDA adapters, RFID readers, and GPS modules.

www.toradex.com **TORADEX**

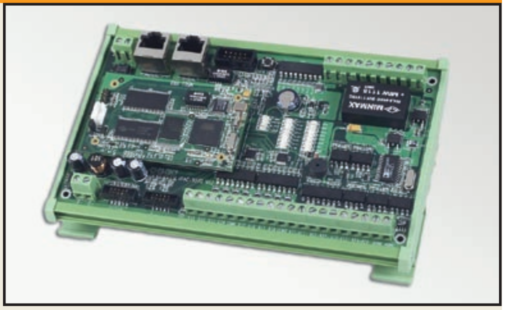
PCI Express XMC module



Innovative Integration's X5-COM is an XMC module with four serial ports directly connected to a Virtex-5 SXT or FXT FPGA computing core, 512 MB of DDR2 DRAM memory, and an eight-lane PCI Express host interface. It has four communications ports: Gigabit Ethernet, Aurora, InfiniBand, and Serial RapidIO, which requires supporting IP in FPGA. Industry-standard SFP modules support up to 4.125 Gbps over copper or fiber-optic cables, where rates depend on FPGA speed and cable. Equipped with 4 MB QDR-II SRAM for computations and four RocketIO links for data planes using P16, the 2.95" x 5.91" (75 mm x 150 mm) module features conduction cooling and thermal monitoring. It can be easily adapted to desktop, CompactPCI, cabled PCI Express, and other systems.

www.innovative-dsp.com **INNOVATIVE INTEGRATION**

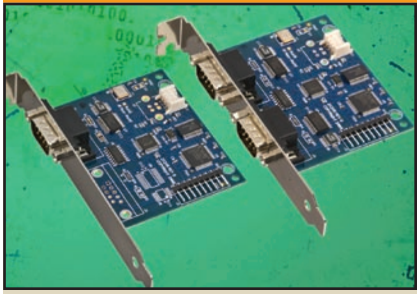
Compact ARM9 SBC



Artila Electronics' iPAC-5070 is a 180 MHz ARM9-based SBC with advanced data acquisition capabilities. The board measures 6.30" x 4.09" x 1.26" (160 mm x 104 mm x 32 mm) and offers 64 MB SDRAM plus 16 MB flash. Equipped with four channels of 16-bit sigma-delta A/D, the iPAC-5070's fully isolated design allows accurate measurement within harsh and noisy environments at an operating temperature of 0 °C to +70 °C. The SBC features industrial DIN-rail mounting along with four channels of isolated 16-bit multiplexed analog inputs, eight channels of opto-isolated digital inputs, eight channels of 500 mA high-drive output, two 10/100 Mbps Ethernet ports, one RS-232 and one RS-485 port, two USB 2.0 host ports for add-on functions, and one SD memory card slot for storage expansion.

www.artila.com **ARTILA ELECTRONICS CO., LTD.**

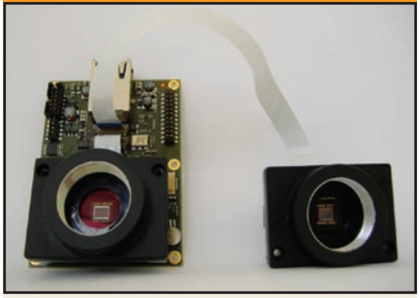
USB-to-serial adapters



Sealevel Systems' SeaLINK/PC.SC (one-port) and SeaLINK+2/PC.SC (two-port) embedded USB-to-serial adapters with a PC bracket can be used to add serial ports to any PC using an internal USB connection. The standard operating temperature range is 0 °C to +70 °C, and extended temperature range (-40 °C to +85 °C) models are available. The adapters offer software-configurable RS-232/422/485 serial ports and automatic RS-485 enable/disable while supporting data rates to 921.6 Kbps. DB9M connectors with full modem control signals are implemented in RS-232 mode.

www.sealevel.com
SEALEVEL SYSTEMS, INC.

High-performance smart cameras

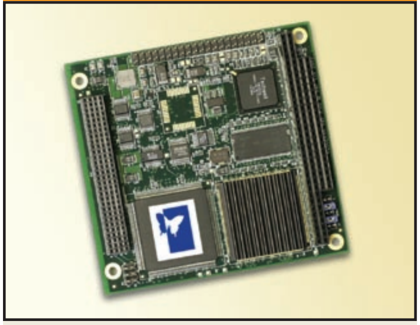


Vision Components' VCSBC64xx family of single board stereo smart cameras from targets 3D machine vision and robot applications. Measuring 2.4" x 4" (60.96 mm x 101.6 mm), each smart camera has an industrial rugged design with two fast image sensor heads and two programmable fast triggers. The VCSBC64xx family operates with an internal, real-time, multitasking operating system and provides 7,200 MIPS of computational power. Insensitive to shock and vibration, the smart cameras offer 256 MB RAM, 16 MB flash, and GbE.

www.vision-comp.com
VISION COMPONENTS

Continued on page 4

H.264 codec on PC/104-*Plus*



Advanced Micro Peripherals' VCODEC-H264 is a single-channel H.264 codec on a PC/104-*Plus* form factor. The board captures high-quality real-time video and audio for H.264 compression and offers an additional path for uncompressed video. It also allows for simultaneous decompression and replay of recordings from storage to the host system's display. Maximum decoded video image size is 720 x 480 (NTSC) or 720 x 576 (PAL). The VCODEC-H264 is available in a -40 °C to +85 °C extended temperature option with +5 V at less than 1.75 A power supply.

www.ampltd.com

ADVANCED MICRO PERIPHERALS, LTD.

Ethernet media converter

The MPL TX2FX is an Ethernet media converter that translates transmission signals from a twisted-pair 10/100/1000BASE-TX to a 100/1000BASE-X fiber-optic cable. It expands network data transmission distances beyond the 100 m limitation of copper wire to more than 10 km using single-mode fiber-optic cable. The SFP transceiver module allows users to select the appropriate module required for the optical interface. The TX2FX features a single-wide power supply input at 5 V to 28 V. An -40 °C to +85 °C extended temperature option is available.

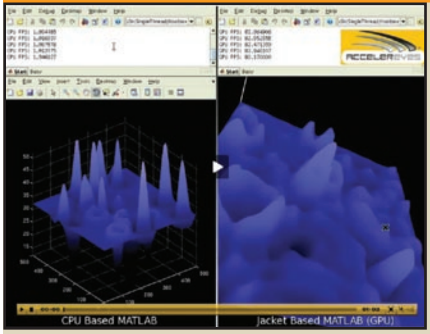
www.mpl.ch **MPL AG**

SAFE33/50 storage enclosure

The MobileSTOR MS2UT+ from Sans Digital is a two-bay external hard drive enclosure with two hot-swappable 3.5" hard drive trays as well as USB 2.0 and eSATA host interfaces. With 3 TB maximum capacity, this 8.0" (D) x 4.8" (W) x 4.0" (H) (203.2 mm x 121.92 mm x 101.6 mm) storage unit uses the latest Silicon Image 5744 chipset supporting RAID 0, RAID 1, spanning, JBOD, SAFE33, and SAFE50. In contrast with SAFE (RAID 1) mode, SAFE33 and SAFE50 create two hard drive volumes where one-third or one-half of the hard drive volume is used for mirroring and the rest is used for spanning. MS2UT+ also offers removable trays for fast access to additional hard drives and a temperature-controlled cooling fan for quiet operation.

www.sansdigital.com **SANS DIGITAL**

Speedy GPU engine for MATLAB



Jacket from AccelerEyes is a GPU engine for MATLAB that enables standard MATLAB code to run on the GPU, connecting MATLAB directly to the speed and visual computing capability of the GPU. Jacket is a complete and transparent system that automatically transfers memory and executes optimization decisions. Using a compile on-the-fly system, GPU functions can run in MATLAB's interpretive style. Built on NVIDIA's CUDA technology, Jacket includes the Graphics Toolbox for MATLAB, which integrates the Jacket computational engine with the full OpenGL capabilities of the GPU. The coupling of computation and graphics allows users to develop true visual computing applications. New features in the Jacket v1.0 release include simultaneous for-loops on the GPU, trace saving, subscripting on logical data, and a new FDTD example.

www.accelereyes.com **AccelerEyes**

Lightweight radio test set

Aeroflex's 3500A is a lightweight 1 GHz handheld radio test set upgraded from the previous 3500 model, with improved audio analysis, integrated audio test connections, and a new microphone interface for easier operation. It weighs less than 8 lbs, offers five hours of battery life with continuous use, and includes a spectrum analyzer with less than -136 dBm noise floor. Able to operate at -20 °C to +50 °C, the 3500A meets MIL-28800F Class II specifications for humidity, altitude, shock, and vibration and can support P25 testing as additional features are added. The unit includes testing capabilities for AM and FM radio systems including power measurements, RSSI, frequency error, FM deviation, AM modulation index, SINAD, distortion, and AF level.

www.aeroflex.com **AEROFLEX**

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Rugged SFFs for vehicles

By Don Dingee, Contributing Editor

A vehicle in today's environment can be almost anything from a fully rugged land combat vehicle to an Unmanned Aerial Vehicle (UAV) or helicopter to a marine vessel. The degree of harshness a computer must endure varies, as do the types of interfaces the platform needs to support. Several examples show the range of Small Form Factor (SFF) platforms designed for today's vehicle-based needs.

Digital Systems Engineering VMC-10

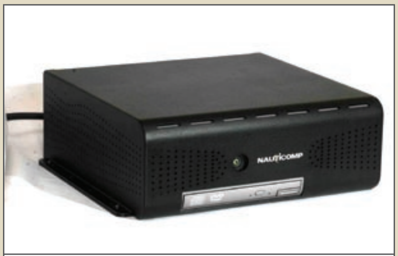
The VMC-10 mobile computer from Digital Systems Engineering (Scottsdale, Arizona, www.digitalsys.com) provides a ruggedized platform with quick-release mounting. Targeting applications like electronic flight bags, sea-based vehicles, and vehicles used for aircraft maintenance, the platform combines ruggedness with fanless operation of an Intel Celeron M processor, memory, and disk drive. Open interfaces like LVDS, Ethernet, and USB fill out the 5.5 lb. package.

General Micro Systems S702

Smaller and more rugged is the General Micro Systems (Rancho Cucamonga, California, www.gms4sbc.com) S702, which GMS CEO and founder Ben Sharfi likes to call "the most powerful processor for its size and weight available." At 5.25" x 5.25" x 2" and 2.5 lbs., with a fanless 2.16 GHz Intel Core 2 Duo and chipsets inside, he might be right. Interfaces include SATA, dual GbE, graphics, USB, and a Mini PCI socket for user I/O. Sharfi indicates that units are undergoing test drives at facilities in Aberdeen and Fort Huachuca in a couple of unnamed vehicle applications. Something this small could certainly go on most UAVs.

Azonix BattleTRAC

Another platform targeting land vehicles is the Azonix (Houston, Texas, www.azonix.com) BattleTRAC. It's a fully functional computer with processor, USB, Ethernet, graphics, audio, and more. It comes in a tough box sealed to IP54 watertight protection and engineered to MIL-STD-810F testing for shock, vibration, and environmental protection. But the interesting features are the vehicle-specific wrinkles. The platform is designed with a modular I/O panel to avoid rewiring vehicles by matching the panel to the application. It has dedicated DC input filtering and conditioning to guard against things like load dumping, jump starting, and other inductive transients in vehicle electrical systems. The unit also has a run-on timer to keep it going after the driver has left the vehicle, perhaps while uploading or downloading data.



Nauticomp NINA

In a different direction aimed at marine navigation is the Nauticomp (Lindsay, Ontario, Canada, www.nauticomp.com) NINA processor. These SFF systems contain boards and components treated with VCI-III corrosion-resistant coating to provide water and salt spray resistance. The boards are then shock-mounted inside the chassis to form a semi-rugged unit. All the usual desktop features are there – Intel Core 2 Duo processor, SATA hard drive, DVI-I video output, GbE, USB, and even a three-year onsite limited warranty from Dell. These are probably not full MIL-SPEC capable, but certainly can serve the needs for commercial or personal maritime craft.

Raytheon Solipsys iTAC

In a portable application intended for the war fighter's or first responder's pocket is the Raytheon Solipsys (Laurel, Maryland, www.solipsys.com) iTAC solution. Using a wireless handheld PDA like the HP iPAQ, iTAC provides real-time access to vehicle and sensor data, along with high-resolution maps, weather information, and more to deliver a full situational awareness picture into the hands of those who need immediate feedback. The device fits within an open architecture framework gathering information from C4ISR data feeds and is designed to download the application over a secure VPN, so nothing needs to be installed or maintained on the PDA.

While we often think of rugged boxes as big, armor-plated behemoths, this sample shows the range of innovative technologies being designed into SFF platforms. Putting the right amount of compute power in the right space is making vehicles smarter, getting information into the right hands faster, and creating better experiences for users.

Fanless EPIC system

AR Infotek's Pipal 2025 is an EPIC embedded system that supports add-on PC/104 modules and provides ultra-low power consumption via its AMD Geode LX800 500 MHz processor. The unit features a fanless platform with a 90° perpendicular I/O design, 9 V to 36 V wide range power supply, and onboard 266/400 MHz DDR memory up to 512 MB. With support for a 4/5 resistor-type touch screen, Pipal 2025 offers USB 2.0, RJ-45 LAN, and DB9 RS-232/485 interfaces and operates at 0 °C to +60 °C.

www.arinfotek.com.tw
AR INFOTEK INC.

Ultra-small IPsec toolkit

The Mocana NanoSec is a standards-based, full-featured, RFC-compliant IPsec toolkit for securing voice, video, and data communications. The micro-footprint, high-performance toolkit requires 65 KB of ROM and is available for more than 100 processor/OS combinations, with ports to new platforms typically completed in two hours. Offering granular IPsec feature controls and advanced cryptography algorithm support, the toolkit can be used to control Internet Key Exchanges (IKEs) and noncompliant security policy packets. The zero-threaded asynchronous architecture supports IKE v1/v2, MOBIKE, PF_KEY interface, XAUTH, ModeConfig, and nanoEAP for EAP authentication.

www.mocana.com **MOCANA**

Robust TFT LCD monitor

Advantech's FPM-5171G is a 17" SXGA industrial monitor with a resistive touch screen. The color TFT LCD flat-panel monitor features Direct-VGA and DVI-D signal transmission and an on-screen display function that allows users to adjust images on the screen. FPM-5171G offers resolution up to 1,280 x 1,024, lockable OSD keys with two user-defined contrast/brightness settings, front-accessible USB connector, combo RS-232 and optional USB interface for a touch-screen function, 10 VDC to 30 VDC power input, and 0 °C to +50 °C operating temperature. The 18.9" x 14" x 2.3" (481.9 mm x 355.9 mm x 58.5 mm) monitor has a robust design with an antirust chassis and an aluminum die-case NEMA 4/IP65-compliant front panel. Supported mounting types include panel, wall, desktop, VESA arm, or 19" rack mount.

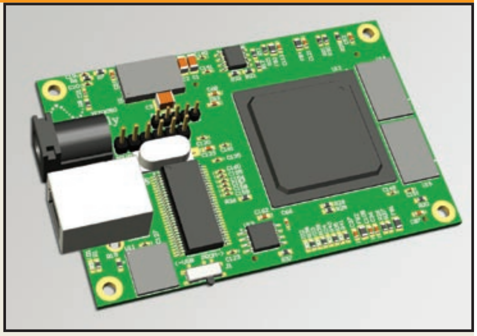
www.advantech.com/ea **ADVANTECH eAUTOMATION GROUP**

Low-power COM Express

The conga-CA945 from congatec is a COM Express-compatible module based on the Intel Atom processor N270 and the full-featured Mobile Intel 945GSE Express chipset in conjunction with the Intel I/O Controller Hub 7-M. The Intel Graphics Media Accelerator 950 integrated in the Mobile Intel 945GSE Express chipset allows for more than 10 GBps bandwidth to a maximum of 224 MB video memory allocation, providing power-efficient 32-bit 3D graphics. Two SATA drives can be connected as fast mass storage devices, and parallel ATA is available to support CompactFlash cards. The conga-CA945 has eight USB 2.0 ports, three PCI Express lanes, one EIDE, PCI, and I2C. Measuring 3.74" x 3.74" (95 mm x 95 mm), the module's low power consumption and ACPI 3.0 battery management make it suitable for mobile embedded applications.

www.congatec.us **congatec AG**

Spartan-3 FPGA integration module



The Opal Kelly XEM3050 is an FPGA integration module based on a 4 million gate Xilinx Spartan-3 FPGA. In addition to the high gate count FPGA, XEM3050 utilizes the high transfer rate of USB 2.0 for configuration downloads, enabling quick FPGA reprogramming. Featuring 64 MB 2x16-bit wide SDRAM and 8 Mb nonvolatile flash, the module is designed to be fully compatible with XEM3010 expansion connectors. An onboard clock generator offers three independent phase-locked loops and five outputs for the FPGA, SDRAM, and expansion connectors. Measuring 2.95" x 1.97" x 0.63" (75 mm x 50 mm x 15.9 mm), XEM3050 can be added to a new board design to provide turnkey USB integration. A DC power jack (P1) and expansion connector (JP3) provide regulated voltage of 4.5 V to 5.5 V.

www.opalkelly.com **OPAL KELLY**

Rugged SFFs for spaceflight

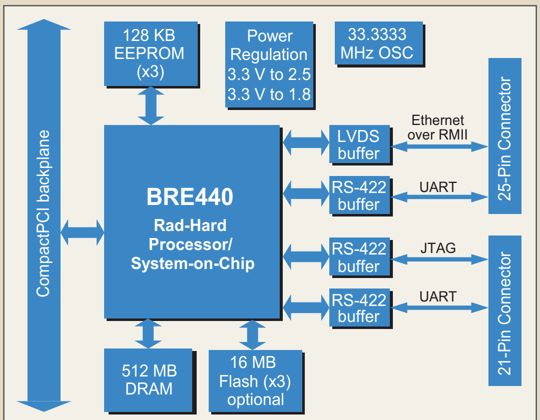
By Don Dingee, Contributing Editor

Turning attention to three examples of rugged SFF computers for spaceflight, these appear to be dominated by Power Architecture processors, FPGAs, and VxWorks operating system support. Also of note in these applications is the use of SpaceWire, a nine-pin serial interface defined by the European Space Agency (similar to IEEE 1355) but gaining use in space programs worldwide.

First, the Application Independent Processor from SEAKR Engineering (Centennial, Colorado, www.seakr.com) is a 7.8" x 11.41" x 10", 18 lb. platform with both a Power Architecture computer board and a reconfigurable computing board with three Xilinx Virtex-4 parts. Flying on the Air Force Research Laboratory's TacSat-3 program later in 2009, the unit processes hyperspectral imagery, pulls targets from queues, and updates war-fighter info via downlink in real time. It has mezzanine-based I/O for interfaces like Camera Link and SpaceWire and is supported with VxWorks.

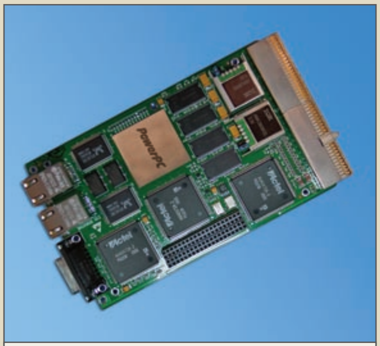
SEAKR Engineering Application Independent Processor

Next, a brand-new System-on-Chip (SoC) and processor board are taking shape at Broad Reach Engineering (Tempe, Arizona, www.broadreachengineering.com). BRE has licensed IBM's PowerPC 440 core and designed it into a purpose-built 1 MRad total dose (TID) hardened SoC, which in turn serves as the processor on the company's Mirideon SBC coming later in 2009. In a 3U CompactPCI format, Mirideon has 10/100 Ethernet and RS-422 interfaces and is supported with VxWorks. BRE is keeping the base computer simple and looking at I/O like SpaceWire and sensor interfaces on additional 3U boards.



Broad Reach Engineering Mirideon

Finally, the Space Micro Inc. (San Diego, California, www.spacemicro.com) Proton400k SBC is in a CompactPCI 3U or 6U form factor. The latest version of the board is designed with a Freescale P2020 processor – not rad-hard itself, but mitigated with patented technologies like time-triple modular redundancy for Single Event Upset (SEU) mitigation and H-Core for Single Event Functional Interrupt (SEFI) mitigation – with a complement of Actel FPGAs. The board is supported under either Linux or VxWorks, with multiple I/O options including PCI Express, SpaceWire, RS-422, and more.



Space Micro Proton400k

Leveraging rugged SFFs to power wearable technology

By Mike Southworth

Mounting a full-function computer on a person takes the right blend of miniaturization and ruggedization, along with a vision for functionality and usability. This application shows the technology and thinking behind a wearable unit used in today's military programs.

The interaction between humans and computers is a subject that has captured the imagination of filmmakers, writers, and scientists alike. The idea that computers can become so tightly integrated into our lives that we hardly notice their presence is no longer reserved for science fiction, but rather is quickly turning into reality.

Seamlessly assimilating this human-computer interaction is the concept behind wearable computers. Different from mobile devices, wearable computers are targeted for applications that require computational support while the user's hands, voice, eyes, and mind are actively engaged in the physical environment. Wearable computing gives military programs the freedom to equip soldiers with wearable networks that create a competitive advantage in network-centric warfare.

Actualizing network-centric warfare

The DoD's net-centric military strategy aims to create a robustly networked force with improved situational awareness and thus mission effectiveness. In net-centric operations, every soldier, weapon, and vehicle becomes a node on a massive tactical information network through wireless connectors. The U.S. military sees net-centric operations as a compelling mechanism for coordinating diverse resources in field operations. This immense data sharing enables field and strategic commanders to obtain real-time situational awareness for tactical planning, give deployed units immediate access to intelligence information, and track both troop and enemy movement across an entire battlefield.

This net-centric approach proves that computers are playing an increasingly critical role on the battlefield. Wearable computing technology provides soldiers with the computing power needed for combat, thereby increasing the success of net-centric warfare.

Only one piece of the puzzle

In their own right, wearable computers provide a vital technology for improving mission effectiveness and troop safety. However, the value of wearable computers depends on the functionality and ruggedness of the networking equipment deployed across the rest of the battlefield.

For example, computers and network equipment in military vehicles, aircraft, and mission control centers are used to create an accurate analysis of a current battlefield situation. To achieve success in net-centric warfare, battlefield networking equipment must meet the following criteria:

- Ruggedized to handle temperature extremes as well as severe mechanical shock and vibration
- Portable enough to address space and weight concerns
- Compatible with a wide range of communications platforms, including wire-line, spread-spectrum RF, optical, and satellite links
- Based on COTS technology to meet the modern military's budget constraints

To ensure that each piece of the net-centric puzzle meets these rigorous requirements, Parvus developed a line of ultra-rugged COTS vehicle mission computers and IP network routers and switches for demanding military programs.

For example, the DuraMAR ruggedized Mobile IP access router (Figure 1) is based on a PC/104 stacking architecture with Cisco IOS routing. The router includes an isolated MIL-STD-704 compliant power supply that accepts a wide range of input DC and provides isolation against voltage spikes and transients experienced by military aircraft and vehicles.

Figure 1 shows the DuraMAR Mobile IP access router based on a PC/104 architecture with Cisco IOS routing.

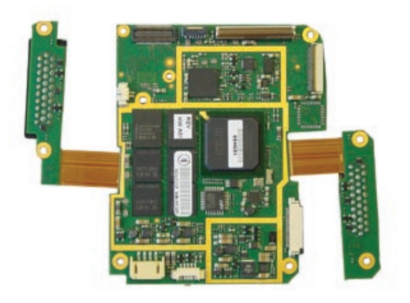
Because a router by itself is not enough to provide a network link, the ruggedized subsystem supports a distributed architecture that enables peripheral devices to be connected, offering radio and other communications links as well as end-user nodes. This architecture uses Power over Ethernet (PoE) and Power with Serial (PwS) to supply power to these peripherals.

Designed for mission operations

In a parallel development, Eurotech created the wearable Zypad WL1000 computer (Figure 2) with the goal of designing a product that completely integrates itself within users' personal space without monopolizing their attention and at the same time gives them computer access without interrupting their activities.


The Zypad WL1000 pictured in Figure 2 gives users quick and easy computer access.

Creating this wearable computer required designers to overcome many significant technological challenges. Studies on ergonomics highlighted the importance of weight, wearability, and screen size in a wearable electronic device. To satisfy these prerequisites, designers miniaturized the computer's circuit card assemblies to make it easy to use and comfortable to wear. Designers used stacked PCBs connected with rigid flex circuits (see Figure 3) to integrate functionality, including all the antennas for GPS, Wi-Fi, and ZigBee.



As shown in Figure 3, flex circuits connect stacked PCBs to incorporate wireless functionality in a wearable computer.

The latest rugged version of the Zypad, the WR1100 (Figure 4), is designed to meet MIL-STD-810F environmental and MIL-STD-461E EMI requirements, making it suitable for military, homeland defense, first responder, security, emergency service, and in-vehicle applications.

This device was designed specifically with soldiers in mind, offering the following enhanced features:

- **Mission mode:** With the mode selector, users can change the device's configuration from normal to mission mode. In mission mode, the user cannot inadvertently switch off the unit. The selector also exposes a programmable alarm button that can be programmed to perform special functions such as erase memory, turn off the LCD backlight, switch off radios, or send a distress call acting as a locator beacon.

Figure 4 displays the latest version of the Zypad, the WR1100, designed to meet strict military requirements.

- **Biometric fingerprint sensor:** By identifying the user, this sensor protects the unit from unauthorized access. In normal mode, users can access the common menu, but only authorized users can access info while the device is in mission mode.

- **Wi-Fi, ZigBee, and Bluetooth wireless connections:** These standardized wireless technologies provide users with options depending on data transfer size and number of nodes.
- **Accelerometer:** The patented orientation sensor saves battery power by changing the system to standby mode when the user lowers his/her arm.
- **Modular expansion:** An integrated, hot-swappable 12-channel GPS receiver module or custom I/O module enables the system to handle specialized I/O or communication requirements (such as 3G or WiMAX) in the field.

Outfitting civil defenders

Intelligent wearable technology that can exchange data in real time under extreme conditions is no longer a goal for the future, as evidenced by the recent deployment of the Zypad in the Civil Defense Unit of Friuli-Venezia Giulia, Italy. Italian civil defense operators are outfitted with a fully wearable and noninvasive computer system for computation and communications purposes in extreme conditions. The uniform for the Italian Civil Defense Unit integrates health monitoring sensors, a helmet fitted with day/night-vision video cameras, and the wrist-worn computer. This technology allows the civil corps to work hands-free, simultaneously communicating and exchanging multimedia data with the command and control center.

The objective of this project is to improve safety for squad members in the field and equip them with their own mini command and control center to receive in real time all multimedia information (maps, videos, information, and audio) needed to optimize mission coordination and management. In addition, the new uniform is fitted with internal sensors that continuously monitor emergency workers' vital physiological traits, recording heart rate, body temperature, hydration levels, and overall health status.

All the devices and their functions are coordinated through the wearable computer, on which images and data can be seen and transmitted to the emergency dispatcher. An integrated GPS system pinpoints the wearer's exact location and generates a map of the area.

Besides the Italian Civil Defense Unit, several U.S. prime defense contractors are currently evaluating the role of wearable computers in various programs. Some think these computers will greatly empower commanders and war fighters with actionable knowledge that can provide a strategic advantage for network-centric operations. Others view wearable computers as more ergonomic or functional replacements for the rugged PDAs or tablet PCs used today.

Beyond military applications

The most challenging aspect of designing wearable technology is concentrating the calculation power and multimedia applications in a unit small enough to be worn by the user. This is where Small Form Factors (SFFs) play a critical role in making wearable technology possible. In addition, wearable computers take advantage of the constant innovations in COTS technologies being developed for portable consumer electronics.

While hundreds of wearable computers are already deployed in homeland security and military applications, technological advancements are making these devices more practical for a host of industrial applications that can benefit from hands-free computer access and a constant network connection. Nonmilitary deployments include the following application areas:

- **First responder:** In emergency situations, wearable computers can help coordinate teams and rescue workers by permitting on-scene workers to exchange information in real time and locate workers' exact locations.
- **Health care:** Wearable computers can provide medical personnel and paramedics with real-time updates on patients' clinical status. In addition, medical staff in first aid situations can have wireless connections to the ambulance, which can then communicate with the control center via radio. This allows

medical staff to exchange information with the control center directly from the emergency site while maintaining contact with the patient.

- **Logistics:** Wearable computers can save time by simplifying inventory tasks, goods sorting in courier hubs, and pickup and delivery from express couriers (see Figure 5).

Wearable computer technology can be useful in industrial applications such as inventory handling, depicted in Figure 5.

Future possibilities

The military's demand for wearable technology is steadily increasing, especially with programs such as the Future Force Warrior of Future Combat Systems and others pushing technology advancement forward. Recent market research indicates that wearable computers are expected to surpass the early adopter phase and become more widely deployed in the next 4-8 years.

Wearable technology architecture may soon be based on new lower-power Intel CPU architectures. This development would provide more processing power while improving operating system compatibility and allowing the device to work with additional operating system types. Wearable computers are quickly proving that the world of computing has the potential to profoundly influence the way we interact with technology.

***Mike Southworth** serves as director of marketing for Salt Lake City-based Parvus Corporation, a manufacturer of rugged COTS computing and IP networking subsystems for military and aerospace applications. In his role at Parvus, Mike oversees the product management and marketing communications programs. Mike holds an MBA from the University of Utah and a BA in Public Relations from Brigham Young University.*

Parvus
801-433-6331
msouthworth@parvus.com • www.parvus.com